Second-order Oversampled Delta-sigma Analog to Digital Converter

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ABSTRACT

The Delta Sigma modulation technology has been around for a while, but because of technological advancements, the devices are now more widely used and feasible. The work proposes a multi-bit Delta Sigma ADC of second order havinga very low power consumption. MATLAB Simulink is used to develop both the Delta Sigma ADCs of first and second orderand the digital output is passed through a digital filter to recreatethe original signal. According to simulation results, at 100 KHz frequency of output sampling, the Delta-Sigma modulator exhibits a Spurious Free Dynamic Range of 95.38 dB, and also it demonstrates that the designed Delta-Sigma ADC is capable of achieving an ENOB (Effective Number of Bits) of 11.83 bits and an SNR of 72.99 dB.

Keywords: Delta Sigma, ADC, Second order

1 Introduction

For the last ten years, there has been a great need for converters from analog to digital (ADC). Typically, ADCs have to be used to bridge the analogous signals with the digital realms. To satisfy these applications, a variety of ADC architectures are generally available. However, the application and its requirements determine which ADC should be chosen. However, not all applications can be served by a single ADC design. The Delta Sigma modulator provides a way to convert data at high resolution while still operating at a faster rate. Oversampling ADCs employ additional DSP functions foranalog to digital conversion when analyzed with Nyquist-rate ADCs. Furthermore, unlike ADCs with a Nyquist frequency, oversampling Delta Sigma A/D converters tend to be unlikely to require steep roll-off antialias filtering. In mixed-signal architectures, sigma-delta modulations are a reliable method for building high-resolution analog-to-digital converters [1].

The necessity for superior definition analog-to-digital converters (ADCs) rises with technological advancement. Sigma- d high accuracy lace speed with precision while requiring fewer fundamental elements by combining the oversampling strategyand the noise-shaping mechanism, in contrast to typical ADCsthat require high-accuracy building blocks. By doing this, an operation that is comparatively impervious to flaws in analog circuits can be gained at the cost of a more sophisticatedand faster digital circuit [2], [3]. The process of converting basic analog pulses to digital information becomes a difficult issue in the era of digitalization since the recording, analysis, and distribution of signals are all done electronically. The ability toexecute conversion utilizing converters such as ADC and DAChas transformed the way that signaling is done Particularly in the electrical and electronic engineering field [4], [5]. It may be stated that the SFDR, SNR, and ENOB performance obtained satisfies all the major requirements for data acquisition systemsfor aerospace applications like launch vehicle telemetry and is on par with those reported in previous publications.

The following is how the paper is set up: Section II discussesthe fundamentals of the Delta Sigma ADC, while Section III includes details of the design architecture of order I, and Section IV includes Order II Delta Sigma ADC. Segment IV indicates the Modelling Results, and Segment V presents the conclusion.

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2 Delta Sigma ADC

The schematic model illustrating a Delta Sigma Analog to Digital converter is displayed in fig. 1. It is made up of a decimation filter and a sigma-delta modulator. The analog- to-digital transition process would have been completed by realizing the modulator using an analog approach to generate a specific bit output, as well as a multi-bit digital stream has been generated by the decimation filter.

Delta-Sigma modulation theory underlies the functioning of the Delta Sigma ADC. Using pulse-density modulation, the Delta Sigma modulation converts high-resolution signals into lower-resolution signals. Much faster compared to the Nyquist

frequency, it samples the supplied pulse. The Delta Sigma ADC's core is the Delta Sigma modulator. It is in charge of digitizing the analogous signal input as well as lowering low-frequency distortions. On this juncture, noise shaping is implemented by the architecture, which causes low-frequency noise to be pushed beyond the region to higher frequencies of interest. Among the causes Delta Sigma converters work effectively with regards to low-frequency, better precision readings are noise shaping.

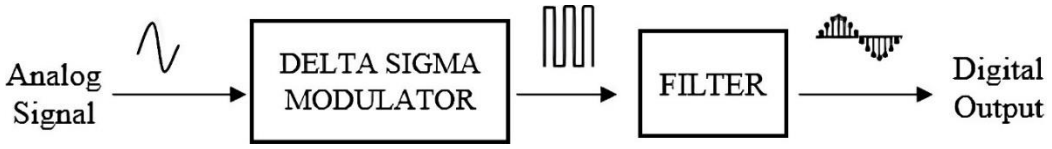

Figure 1: *Schematic model of Delta Sigma A/D Converter*

As a result of sampling with the frequency which will be substantially higher when compared to the bandwidth of the signal, loops of feedback can change quantization disruption thus the majority of those power that noise produces is moved outside the range of the signal. After that, beyond-the-band distortions could have been decreased using any digital filtering method. The ratio of over-sampling and the noise shaping order affects how much the quantization noise can be reduced. When compared to Nyquist-rate architectures, generally the sampling rate is raised to decrease the analog circuits' level of complexity needed. As a result, many signal processing duties may now be moved towards the digital domain, during which energy expenditure could be decreased by effectively resizing device layouts and then could lower the supply voltage [6].

The modulator's 1-bit comparator and the system clockwork together to implement the sampling speed, f_s. In this way, the system clock's high sample rate is used to provide the quantizing regarding the Sigma Delta modulator. The DeltaSigma modulator generates a sequence of digital data that corresponds to the input data, just like all quantizers do. The input analog voltage is therefore represented by the ratio of ones to zeros. The Delta Sigma modulator has an integrator, which is unusual for quantizers and provides the impact of pushing quantization noise towards higher frequency ranges.

The comparator's output value is simultaneously timed back into the DAC and passed through the filtering section consisting of decimators as well. When the comparator's resultant value shifts from one to zero as well as the other way around, The DAC of 1-bit resolution operates by altering the difference amplifier's equivalent output voltage. As a result, the voltage output is altered, which will result in the integrator moving in the other orientation. The input signal at the sampling rate is represented by pulse waves in this time-domain output signal. (f_s). The average output pulse train has the same value as the input signal. The 1-bit ADC digitizes the signal in the time domain to a rough, output code of 1 bit, which results in the converter's noise caused by quantization.

3 First Order Delta Sigma ADC

The Sigma Delta ADC of order I comprises an integrator, a relay, and a sampler in order to perform digitalization of the input analog signal.

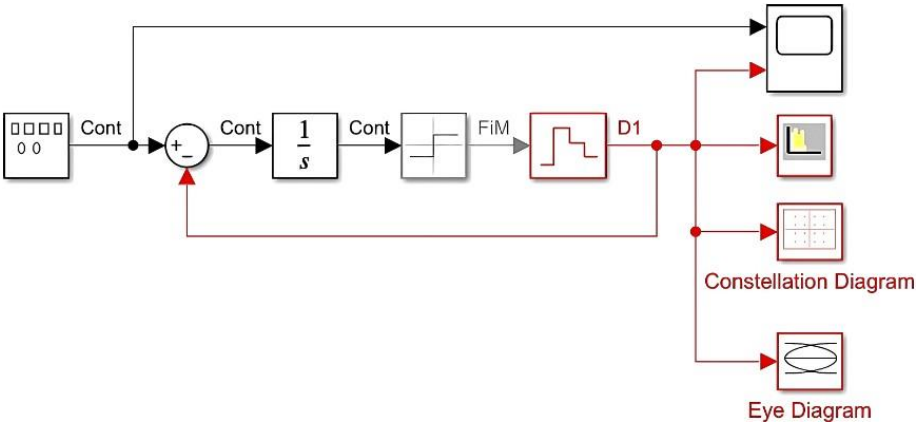

Figure 2: *First Order Delta Sigma Modulator*

The First Order Sigma Delta ADC Simulink model has beendisplayed in Fig. 2. The integrator shapes the noises to high frequency and the corresponding noise is then eliminated by using a filter. A Relay act as a block that converts the continuous analog signal to a discrete signal and there is a block for sampling and holding to adjust corresponding sampling frequency. The best converters for transforming signals with a high level of resolution across a broad frequency band, ranging from dc up to few MHz, are sigma-delta converters.

High quantization noise is a problem for the sigma-delta modulator at high frequencies. This quantization noise needsto be eliminated for the purpose to achieve a greater resolution,and the resulting Delta Sigma modulator's sample rate must be eliminated or dropped off towards the Nyquist rate to minimize the amount of data needed for further distribution, recording, or processing of digital signals.

4 Second Order Delta Sigma ADC

The second-order Delta Sigma modulator's operational structure is shown in Fig. 3 and was created using MATLAB Simulink. Two integrators, two Relays, two Sample and Hold blocks, a summer, and two integrators constitute the second- order Delta Sigma modulator. Only one bit (two levels) of data, or 1 or -1, is included in the modulator output.

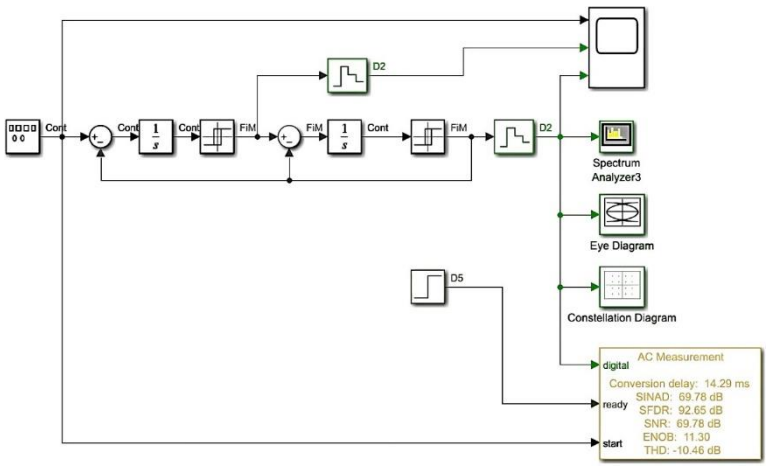

Figure 3: *Second Order Delta Sigma ADC.*

Multi-loop sequential design and single-loop architectural design tend to be the two primary types of sigma-

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delta superior order modulator design structures. Both seem to be complicated in general. Each of the modulator's orders is alongside the high-gain forward path, which implies that the distortion resulting from the non-ideal nature would be transmitted using the precise feedback pathway, making an individual loop modulator's efficiency unaffected by the characteristics of the analog circuitry thus noticeably reducing those demands placed on the analog circuitry. But since the signal relativity alone makes high-order individual loops constrainedly stable [7], the high- order system's equilibrium needs to be thoroughly assessed while processing system design.

It is more accurate to use a Second-order (or higher) Delta Sigma Modulator than a 1st-order Delta Sigma Modulator. It has greater bandwidth and a slower clock rate for processing input signals. The Delta Sigma Modulator of the Second Order whose output signal is substantially more similar to the optimum pulse proportion output signal and has less noise. Delta-Sigma Modulator of order II, in particular, considerably reduces unpredictable noise. The modulator's within the band noise from quantization can be considerably decreased through employing a circuit that integrates twice as opposed to once. The noise element in the II-order modulator is affected by both the prior error and the error before it.

In comparison to lower-order modulators, multi-order modulators can shape quantization noise at higher frequencies. Both the thermal interference as well as quantization distortion have to be decreased in a Delta-Sigma Modulator so as to raise the SNDR. By raising the loop gain inside the signal band, the quantization noise can be reduced.

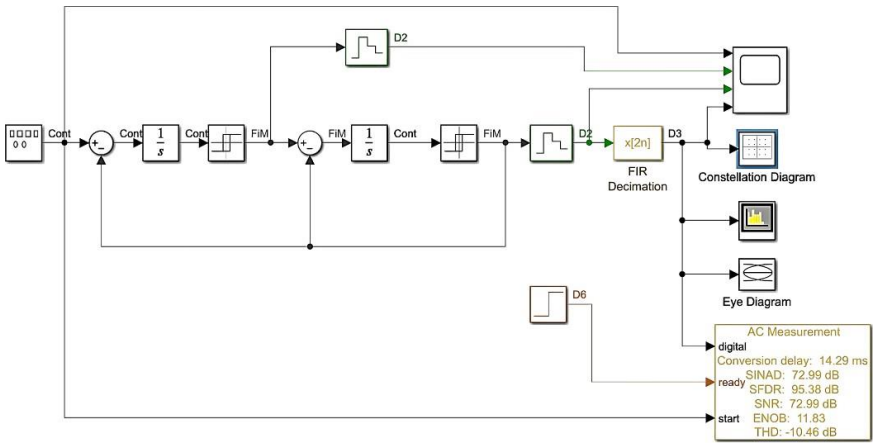

Figure 4: *Second Order Delta Sigma ADC with filter.*

During the conversion procedure, modulator within the Delta Sigma A/D Converter effectively lowers noises at low frequencies. The high-frequency disturbances, on the other hand, remain as an issue and are unwanted inside the converter's outcome, and the FIR filter helps to mitigate this. The Simulink Framework for Second Order Sigma-Delta ADC incorporating the filter section is shown in Fig.4. After implementing the filter section, the SNR has increased from 68.78 dB to 72.99 dB.

5 Simulated Results

The second-order Delta sigma modulator's response considering an input sine wave and at the sampling rate of 100 KHz is depicted in Fig. 5. It is obvious that the result is a pulse- width modulated sine wave that has been matched with relation to the sine wave input. At the input sine wave's positive peak, there are more 1s and fewer -1s, and at the negative peak, the opposite is true. When the amplitude of the input signal is zero, and this is how a Sigma Delta Modulator is meant to react, there are an equal number of 1s and -1s.

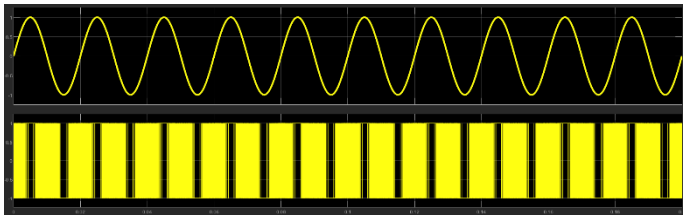

Figure 5: *Digital Output of Second-order Delta Sigma ADC*

The response from a decimation filter is illustrated in Fig. 6. It is obvious that the decimation filter successfully reduces out- of-band noise and boosts SNR. The designed decimation filter in the Delta Sigma ADC performs a low pass filtering duty and reduction of the sampling frequency of the modulator signal.

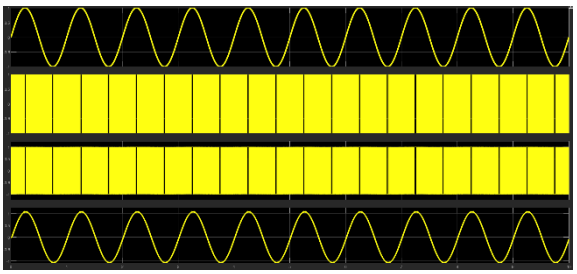

Figure 6: *Output of Second-order Delta Sigma ADC with Filter*

Fig. 7 depicts the frequency response of the FIR filter which is employed to eliminate quantization noise.

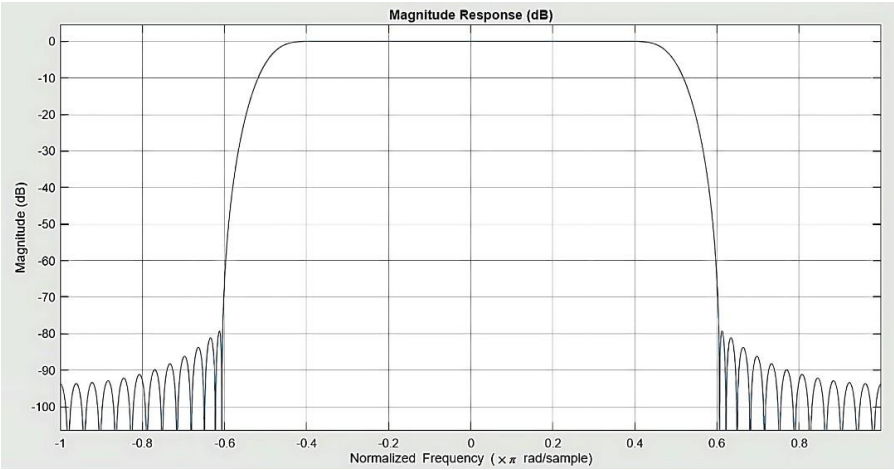

Figure 7: *Frequency response of the filter*

ADCs are used to interface real-world signals with digital processors. For power efficiency and electronic system performance in ADCs, downscaling is a significant issue.

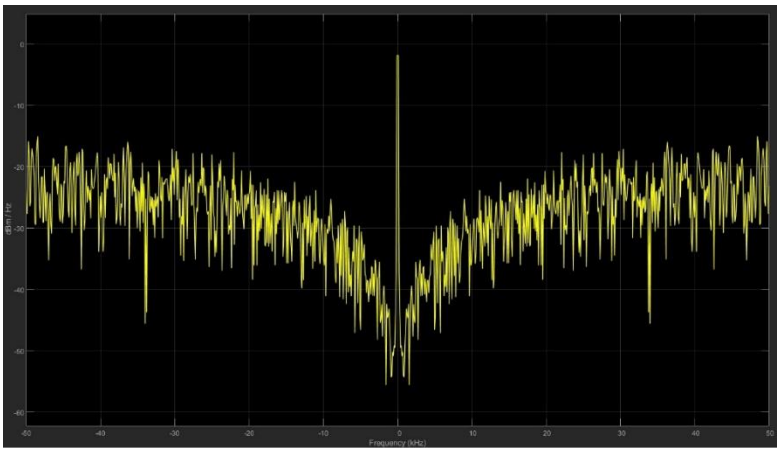

Figure 8: *PSD of the designed Delta Sigma modulator*

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Modeling the Delta sigma modulator of Second order in Simulink gives a Signal to Noise and Distortion ratio of 71.77 dB, a Spurious Free Dynamic Range of 93.61 dB, the Total Harmonic Distortion is -10.46 and a Noise floor of -309.15 dBm as shown in Table 1. The estimated power spectrum density (PSD) of the designed Delta Sigma modulator is illustrated in Fig. 8.

Table 1: *Simulated Results of Delta Sigma ADC*

	Parameter	*Value*
1	Signal to Noise and Distortion Ratio (SINAD)	71.77dB
2	Spurious Free Dynamic Range (SFDR)	93.61dB
3	Signal Noise Ratio (SNR)	71.77dB
4	Effective No. of Bits (ENOB)	11.63
5	Total Harmonic Distortion (THD)	-10.46dB
6	Noise Floor	-309.15dBm

6 Conclusion

In general, a modulator and a digital/decimation filter make up a Delta Sigma ADC. Using a 1-bit ADC, and oversampling, the modulator transforms the analogous input straight up to digital form. The interference-shaping mechanism in the A/D converter architecture is used for shifting the quantization noise from lower frequency ranges toward higher frequencies. The modulator stage's High-frequency interference is eliminated with the aid of low-pass digital/decimation filter, that also lowers the device's output data rate to an acceptable frequency. There is a direct relationship between the resulting rate of data and the resolution of the converter. Lower data rates offer a high effective resolution, or ENOB, at the converter's output if the sample rate is kept constant. The Sigma Delta ADC of II order that is proposed in this work provides an improved SNR of 72.99 dB at a sampling frequency of 100 KHz.

7 Publisher's Note

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References

[1] Boser, B. E. "TheDesign of Sigma-Delta Modulation Analog-to-Digital Converters," IEEE Journal of Solid-State Circuits, Vol. 23, No. 6, pp. 1298-1308 (1988).

[2] BOSERB E. The design of sigma-delta modulation analog-to-digital converters [J].IE EE J Sol Sta Cire, 1988, 23(6): 1298-1308.

[3] BAIRD R T, FIEZ T S. A low oversampling ratio 14-b 500-kHz sigma-delta ADC with a self-calibrated multibit DAC[J].IEEEJ SolSta Circ,1996,31(3):312-320.

[4] Straayer, M., and Perrot, M., "A 12-bits, 10-MHz bandwidth, continuous-time delta-sigma ADC with a 5- bits, 950-MS/s VCO based Quantizer," J. Solid-State Circuits, 2016, 43, (4), pp. 805–814.

[5] Reddy, K., Rao, S., Inti, R., et al.," A 16 mW78 dB-SNDR 10 MHz BW CT- ADC using residue- canceling VCO-based Quantizer," ISSCC Dig. Tech. Papers, February 2012, pp. 152–1536.

[6] Tony Chan Carusone, David A. Johns and Kenneth W. Martin "Analog Integrated Circuit Design", John Wiley Sons, Inc. Second Edition, NJ (2012).

[7] R. Schreier. Understanding Delta-Sigma Data Converters[M].USA; IEEE Press, 2005:91-135.