Study of Scaling Limits of Multi-gate Fets (Finfet) with High-K Dielectric

W. Z. Goh[1], B. Fong[2], H. Hussin[3], S. F. Wan Muhamad Hatta[4*]

[1,2,4]Department of Electrical Engineering, Faculty of Engineering, Universiti Malaya, 50603 Kuala Lumpur, Malaysia

[3]School of Electrical Engineering, College of Engineering, Universiti Teknologi MARA, 40450, Malaysia

[4]Centre of Printable Electronics, Universiti Malaya, 50603 Kuala Lumpur, Malaysia

[*]Corresponding Author

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ABSTRACT

Scaling of Multi-Gate FETs (FinFETs) to sub nanometer has seen several challenging problems such as short channel effects which significantly affect the device performance and huge off-state power leakage. High-k dielectric materials had always been looked at as a potential replacement to the conventional SiO_2 to increase gate control over the channel, which could be a possible solution. This paper examines the impact of scaling FinFETs with varying geometric conditions in the presence of high-k gate dielectrics oxide layer, and further demonstrate conflicting technical trade-off that emerges from short channel effects due to different oxide materials. The electric field distribution, carrier density and mobility of the FinFETs subsequent to miniaturization were also studied. A 3D model of the device is created and simulated using TiberLab and Nanohub to observe the carrier density and mobility in the device as well as the electric field created within the device. Short channel effects specifically drain induced barrier lowering (DIBL) and gate induced drain lowering (GIBL) were also analyzed. The overall results show that although high-k dielectric gate oxide has some drawbacks, it still outperforms SiO_2 overall as a gate oxide material and has been proven to be a solid solution to mitigate short channel effect. The I_{on}/I_{off} for the HfO_2-based device increases by 90% as compared to a SiO_2-based device. However, it was evident that the threshold voltage had increased slightly from 0.13 V to 0.26 V when the dielectric was changed from SiO_2 to HfO_2.

Keywords: High-K Dielectric, Multigate FET (FinFETs), Scaling transistor, short channel effect (SCE), leakage current

1 Introduction

The FinFET is a non-planar three-dimensional dual gate transistor with a fin-like structure and a thin silicon film wrapped over the conducting channel. This structure enables a FinFET to be optimized using different gate oxide material in providing stronger control towards the conducting channel, and ultimately to tackle short channel effects (SCEs). The material of the gate oxide serves a significant role in FinFET design. Different options of high-k dielectric material requisites of a material to act as a better gate oxide than SiO_2 by considering the carrier mobility and leakage current of the present material. Dielectric constant or relative permittivity, k is the material's permittivity (absolute) expressed as a ratio relative to the vacuum permittivity and can also be define as the ability for the material to store charge. The following is an equation for a normalized gate capacitance [1]:

$$C_{ox} = \frac{k\varepsilon_0}{T_{ox}} \quad (1)$$

where ε_0 = permittivity of free space, C_{ox} = oxide capacitance per unit area. Hence, when decreasing the oxide layer thickness is reaching its limitation, theoretically the other way to increase gate capacity is by

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using high-k dielectric. The 'fins' form the source and drain of the transistor and due to this unique structure, the gate can control the channel of the transistor by means of the 3-dimensional fin-like structures of sufficient lengths. FinFETs has substantially lower power consumption as compared to conventional transistors which allows high integration levels on an integrated circuit (IC) [2]. FinFETs also operate at a lower voltage because of their lower threshold voltage with higher operating speed and lower static leakage current. The introduction of FinFET is able solve many problems related to SCEs, due to its electron drift characteristic in the channel and the ability to refine its threshold voltage by shortening of its channel length [3]. With the increasing demand for the reduction of size of electronic component in IC, the world is now currently seeking a solution to increase the number of transistors per unit area, thus integration of FinFETs in modern circuits is paramount.

2 Design considerations of the FinFET

The NanoHub MugFET and Tiberlab simulators were used in this work. Silicon Nitride, Si_3N_4 (ε = 7.5), Aluminum Oxide, Al_2O_3 (ε = 10) and Zirconium Oxide, ZrO_2 or Hafnium Oxide, HfO_2 (ε = 25) were chosen as the gate oxide to be simulated along with the conventional Silicon Dioxide, SiO_2 (ε = 3.9), to understand the effect of high-k materials and find a replacement for SiO_2 in the process of scaling down FinFETs to sub nanometer region. The focus is to reduce the leakage current which is amplified due to constant scaling of the device by replacing SiO_2 with a physically thicker layer of metal oxides with a higher relative permittivity. Figure 1 shows the transfer characteristic of the simulated FinFET device with different gate oxide, and it is apparent that FinFETs with high-k gate oxides display lower off-state leakage current while maintaining the same Ion, thus resulting in higher Ion/Ioff ratio.

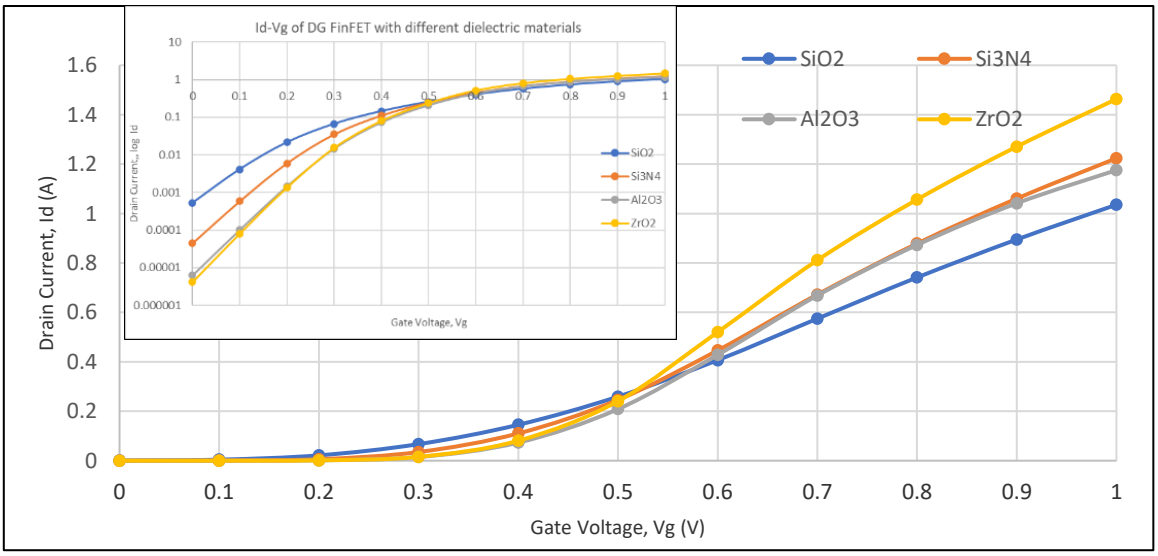

Figure 1: *Transfer characteristic of DG FinFET with different high -k dielectric. Inset shows the leakage current in subthreshold region.*

3 Results and discussion

3.1 Transfer characteristics of FinFET with varying gate length, channel width and oxide thickness

Figure 2 (a) and 2 (b) shows the transfer characteristic of the FinFET with different dielectric materials at varying gate length. It was observed that when the gate length scales down from 40 nm to 20 nm, the off-state current leakage increases drastically.

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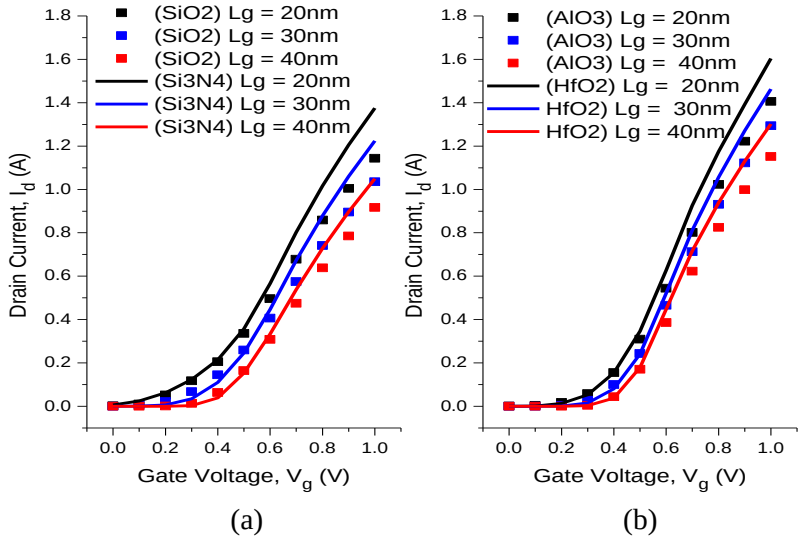

Figure 2: *Transfer characteristic of DG FinFET with varying gate length (a) ε = 3.9 (SiO_2) and ε = 7.5 (Si_3N_4); (b) ε = 10 (Al_2O_3) and ε = 25 (HfO_2)*

It was apparent that the 40 nm gate length has the lowest off-state current leakage while 20 nm has the highest off-state current leakage across all gate oxide graph. To better compare the impact of a high-k material on reducing the short channel effect of the MuGFET, the threshold voltage Vth, off-state leakage current and Ion/Ioff ratio of the 20 nm FinFET are tabulated in the Table 1 below.

Table 1: *Performance metrics of DG FINFET of L_g= 20 nm with different gate oxide*

Dielectric Materials	I_{off} (A)	I_{on}/I_{off}	V_{th} (V)
SiO_2	1.744E-6	5.73	0.094
Si_3N_4	1.0087E-6	9.91	0.107
Al_2O_3	0.687E-6	14.55	0.142
HfO_2	0.0988E-6	101.21	0.188

FinFET with SiO_2 as the gate oxide has the highest off-state current of 1.744 µA followed by 1.009 µA for Si_3N_4, 0.68 µA for Al_2O_3 and 0.099 µA for HfO_2. This significant decrease in off-state current result in higher Ion/Ioff ratio for device with high-k dielectric such as HfO_2 that has an Ion/Ioff ratio of 101.21 which is around 1700% increase compared to SiO_2 and the reason of the decrease in the off-state current is due to the increase barrier potential faced by the carrier when high-k dielectric is utilize as the gate oxide. High-k dielectric provides the gate with better capacitive control over the channel which leads to better on characteristic such as lower subthreshold swing and higher on-current. The high-k dielectric also provides the gate more control to turn off the device, especially at shorter gate length. According to previous reports [4], the maximum drain current scale inversely proportional to the gate length which is exactly shown as the result obtained in this work. This result proves that high-k device can scale better than SiO_2 to shorter gate length before important characteristics such as transconductance, Ion/Ioff, and subthreshold swing are degraded. However, the Ion/Ioff ratio were still considerably low and could do further improvement using Gate Material Engineering (GME) technique or include an interfacial layer of SiO_2 as mentioned by Boucart et al. [4] Combined with the results shown at Figure 2(a) and 2(b), it can be deduced that high-k

improved the subthreshold performance, off-state current leakage and device switching speed of the FinFET by increasing the Ion/Ioff ratio. This is a very essential aspect for low operation device or creating high-powered device with low power consumption.

3.2 Transfer characteristics of FinFET with varying channel width

It is indicated that the on-state current and off-state current decreases as the channel width decreases. From the results obtained, it can be observed that FinFET with channel width, W_{ch} = 20 nm had the lowest off-state leakage current across all gate oxide materials. This trend is mainly because current is proportional to the channel doping concentration and the cross-section of the channel. The Ion/Ioff ratio, off-state leakage current and threshold voltage of the each high-k dielectric is tabulated in Table2.0 below for comparison. From the table, it can be observed that high-k gate oxide FinFET had lower off-state leakage current, higher Ion/Ioff ratio and higher threshold voltage with HfO_2 having the best result. It is also important to note that the threshold voltage reduces when the channel width is decreased because in low doping concentration, Vth variation is not significant. Lower Vth could allow device to be switched off at a lower gate voltage. This is because by shrinking the size of the channel width, the gates get closer to each other and have better electrostatic control on the carriers inside the channel. Although high-k gate oxide (HfO_2) has slightly higher threshold voltage, the increment of 11.13% compared to SiO_2 in Vth is still acceptable considering that the Ion/Ioff ratio increase significantly by 6079%. This is mainly due to higher gate capacitance of high-k gate oxide which resulting in stronger gate control in the channel with bigger depletion region and paired with device with low channel width, minimum leakage current was obtained.

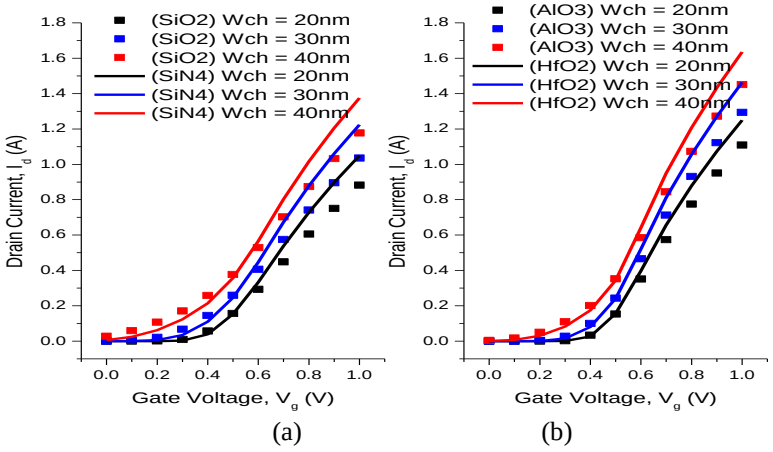

Figure 3: *Transfer characteristic of DG FinFET with varying channel width (a) ε = 3.9 (SiO_2) and ε = 7.5 (Si_3N_4); (b) ε = 10 (Al_2O_3) and ε = 25 (HfO_2)*

Table 2: *Performance metrics of DG FINFET of W_{ch}= 20nm with different gate oxide*

Dielectric Materials	I_{off} (A)	I_{on}/I_{off}	V_{th} (V)
SiO2	1.634E-6	6119.95	0.3010
Si3N4	1.630E-7	61349.70	0.3190
Al2O3	8.544E-8	117041.20	0.3241
HfO2	2.688E-8	372023.81	0.3345

3.3 Quantum mechanical tunnelling and Short Channel Effects in FinFETs

Quantum Mechanical Tunnelling occurs when the gate dimension is so thin that the charge carrier has a certain statistical probability of being able to tunnel through the oxide layer. It can also be calculated

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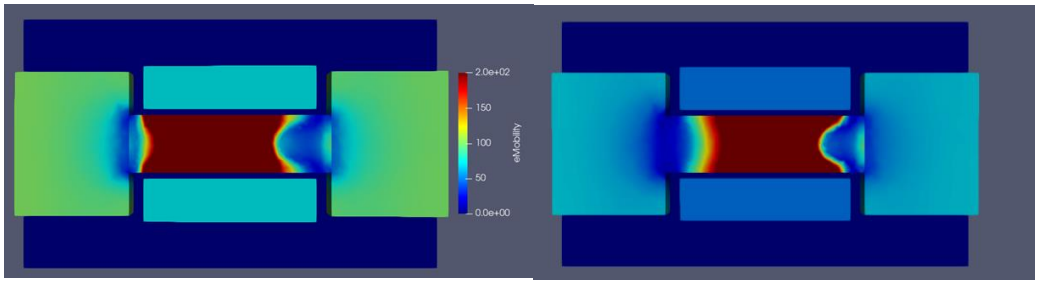
according to the data obtained that when oxide thickness decreases from 5nm to 1nm, leakage current of SiO_2 increases 131% while other high k material had higher leakage increment with 498% of Si_3N_4, 350% of Al_2O_3 and 169% of HfO_2.This is due to higher dielectric constant material has a smaller band gap which causes more tunneling in gate oxide as charge carrier can easily acquire enough energy to bypass the gate oxide. SiO_2 on the other side has a larger band gap hence less tunneling. A proposed structure may be considered by adding a layer of SiO_2 in between the high-k materials and the channel to act as an interfacial oxide which is a buffer layer between silicon substrate and high-k dielectric to improve high-k dielectric and silicon substrate interface quality, the channel carrier mobility and act as the nucleation layer of high-k dielectric deposition [5]. It is shown that the DIBL is highest when SiO_2 as the dielectric materials of the gate oxide and the value reduces when the dielectric constant of the dielectric increases which is further supported by work of [6]. It decreases 40% in FinFET device with HfO_2 as gate oxide. This further strengthen that FinFET with high-k dielectrics could eliminate the leakage current effectively due to less drain induced barrier lowering effect in the nanoscale device. This also shows that high-k materials can mitigate short channel effect in scaling down FinFETs effectively since DIBL is a short channel effect, where high DIBL can reduce the operating frequency of the device due to high drain voltage that would open the depletion barrier prematurely. Other than that, it could be analyzed that with the reduction in the source junction barrier, electrons can inject into the channel easily with the gate voltage no longer has any control over the drain current [7]. The electrostatic potential along the channel is increased for the devices with different high-k materials as gate oxide which contributes to the reduction of DIBL [8].

4 Study of electron mobility for FinFETs of different gate oxides

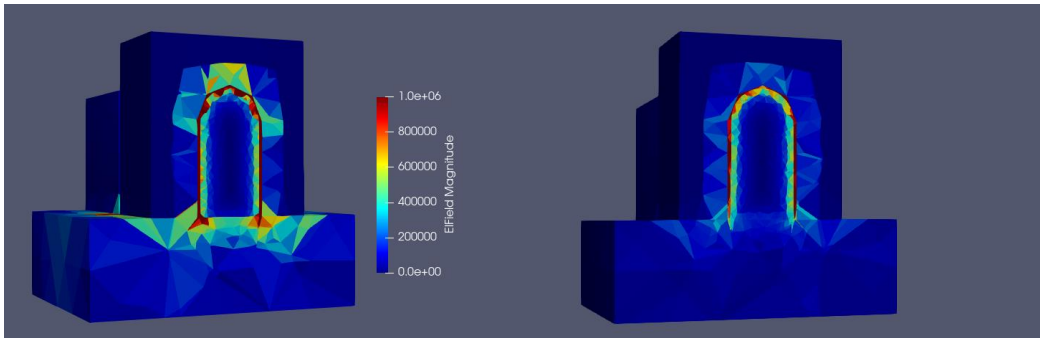
The result of simulation analyses electron mobility and the respective electric field of TG FinFET using each oxide materials with different gate length and oxide thickness were done.



(a) **(b)**

Figure 4 : *Comparison of electron mobility between TriGate FinFET using (a) SiO_2 and (b) HfO_2 as gate oxide using TiberLab 3D simulation*

The speed of a FET device depends heavily on source to drain current which also tightly related to carrier mobility. Higher electron mobility equates to higher source drain current which in return creates faster device. Carriers in FET behave like a 2D electron gas, and the carrier density is determined by the vertical gate field which induces them by Poisson's equation. Firstly, high-k dielectric contains much more trapped charge than SiO_2 and excessive number of trapped charges and interface states causes Coulombic scattering. Other than that, there is high possibility of remote scattering by low lying polar phonon modes as dielectric layer are made up of dipoles that vibrates and lead to high oscillation in the crystal lattice.



(a) **(b)**

Figure 5: *Comparison of electric field generated in TriGate FinFET using (a) SiO_2 and (b) HfO_2 as gate oxide using 3D simulation with oxide thickness of 1 nm*

It is evident that the electric field at drain junction is significantly reduce when gate oxide is switch to HfO_2. This is vital to reduce the Drain Induced Barrier Lowering (DIBL) of the device which generally occurs due to high electric field at drain junction. Significant reduction in source to channel barrier height occur due to high electric field at drain terminal and charge carrier could flow from source to drain continuously which result in sub-threshold leakage current. Threshold voltage of the device decreases in return of higher source-drain voltage when the device is shortened and the source to channel barrier height are reduced and surface potential increases as a result as according to the following:

$$V_{th} = \Phi_{GC} - 2\Phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (2)$$

where, Φ_{GC} = work function difference of gate and channel, Φ_F = Fermi/bulk potential, Q_B = charge of depletion region in the substrate, and Q_{ox} = positive charge density at gate oxide and silicon substrate interface [9]. When source drain voltage increases, the longitudinal electric field in the channel will increase as well and the increasing surface potential causes the vertical electric field to become stronger. This increases the resultant electric field which causes the threshold voltage to reduce and trigger the increasing DIBL. The high permittivity of a high-k dielectric material stops charge carriers to tunnel from channel to the gate region which are accelerated by high work function. The polarized field present in high-k oxide cancelled off the electric field present at the oxide channel region, hence lower electric field at the oxide channel region.

5 Conclusions

In this work, the electrical characteristic and performance of Multigate FinFET device with different geometrical parameters and gate oxide is analysed and compared to FinFET device using typical SiO_2. The effect of replacing SiO_2 with high-k dielectric materials on mitigating short channel effect when scaling down the device in terms of gate length, fin width and oxide thickness were simulated and studied. A 3D model is created and simulated using drift-diffusion method. The output is viewed on a visualization application and thorough analysis is done based on the electric field generated, electron mobility and electron density of the device. High-k dielectric materials significant increases ON current, Ion/Ioff ratio and transconductance of the device. Short Channel Effect of high-k device such as off-state leakage current, gate tunneling leakage current and drain induced barrier lowering can be seen to have reduced significantly when compared to FinFET with SiO_2. Drain Induced Barrier Lowering which occurs due to high electric field at drain junction when the device in significantly reduced when high-k materials is used as the gate oxide.

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6 Declarations

6.1 Acknowledgements

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6.2 Competing Interests

There is no conflict of interest.

6.3 Publisher's Note

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