Design and Performance Analysis of 4-input Multiplexer Tree using FGMOS

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Abstract

The work proposed in this paper presents the design of Ultra Lowpower–Lowvoltage2-input multiplexer using Floating Gate MOS (FGMOS), which is subsequently used to design and simulate 4-input Multiplexer tree. This paper further investigates the performance of FGMOS based Multiplexer tree and its comparison with the conventional CMOS based multiplexer circuit. The FGMOS is a technique that offers variability in threshold voltage with significant adjustment of the bias voltage. Moreover, the current trends in VLSI demands the use of techniques that remain compatible with the decreasing feature size along with increasing density, device reliability and speed by ensuring the less power consumption, low voltage operation and reduction in the overheating, for which FGMOS is a considerable choice. Also, Low voltage circuit techniques plays a vital role in the designing of battery powered mixed signal microelectronic systems. The simulations in the proposed paper are carried out in LTSPICE using TSMC 180nm technology and 1-voltsupply. As compared to the conventional CMOS based 2-input multiplexer, FGMOS based 2-input multiplexer has 84 % lesser power consumption whereas FGMOS based 4-input multiplexer has 70 % lesser power consumption when compared to conventional CMOS based4-input multiplexer which in turn will tremendously reduce the problem of overheating in mux switching devices. It is also observed that as the order of FGMOS based multiplexer is increasing, there is an improvement in the delay, PDP and EDP.

Keywords: Ultra low power; Low voltage; FGMOS; Multi- plexer tree; CMOS; MUX.

1 Introduction

In Digital world, we work with high and low or 1 and 0 logic states. Various digital devices like logic gates, registers, counters, encoders and multiplexers etc. are used for the purpose of manipulating digital signals. Multiplexer also known as MUX is one such digital device that permits numerous inputs and allows anyone out of the given inputs to pass onto the single output line; hence it is also known as a MISO (multiple input single output) device. Output of the MUX is selected on the basis of the select line combination [1]. The demand of faster digital circuits having lesser power consumption is profoundly accelerating due to rapid enhancement of technologies in the field of communication, biomedical systems and battery- operated applications etc. With the continuous reduction of feature size in CMOS circuits and corresponding increment in thechip density, power consumption has become a major concern in VLSI design. This can be successfully achieved by lowering supply voltage (VDD) and threshold voltage (VT) of MOSFETs, but it is quite prominent that scaling down of supply voltage do not lead to proportional scaling of VTof the devices. So, the concept of reduction of supply voltage independent of scaling by use of Floating gate mosfet (FGMOS) came into picture and is utilized in this paper for the significant lowering of consumed power in CMOS circuits. FGMOS technique has perpetually displayed better performance in lieu of conventional CMOS circuits in regards to power, low voltage, output swing etc.[2,3,7]. Features like controllability, flexibility and tunability in FGMOS are successfully exploited in some recent years for better results [5].

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These devices should maintain compatibility with the current fabrication processes of that reduced threshold doesn't impose a constraint on the cost of fabrication[7].

In 1967 "D. Kahng" and "S.M. Sze" introduced FGMOS for non-volatile memory cell application.[7] In Floating Gate MOSFETs [11] V_{TH} depends on the applied control gate voltage and by varying it, V_{TH} can be adjusted as per the requirement which in turn gives extra liberty to exploit the tunability feature of FGMOS.

The FGMOS structure is dependent on standard MOS and CMOS process technology and is fabricated with an additional gate capacitance connected in series with the gate of standard transistor, due to which FGMOS leads to the tuning of threshold voltage required by the transistor to turn ON. This tuning of the threshold is the result of charging of the node present between the additional gate capacitance and the standard MOS gate. It will be known as a true floating- gate circuit when there will be no charge leakage and the extra capacitance added is known as the floating-gate capacitance (C_{FG}). The effective threshold voltage will vary in accordance with the value of Floating gate charge voltage (V_{FG}). The value of V_{FG} is obtained in the design process itself which is then used to design the circuit and is kept fixed throughout the operation [6]. For true floating gate implementation several methods like tunnelling of electron, hot-electron injection, or UV-exposure method are usually used [3].

As per the recent trends, transistor-based designs such as ternary logic gates, comparators, multipliers, cascode amplifiers, Current mode circuits, linear resistance, analog cells such as current mirrors and active building blocks such as operational transconductance amplifier (OTA) are proposed in the literature that uses FGMOS as a replacement of MOS to achieve low power operations[7].

Computational circuits and particularly multiplexer circuits play a vital role in telecommunication applications, medical equipment, hearing devices and memory drives[8].The above- mentioned digital circuits have further application in several important fields such as satellites, military's equipment, in computer, remote controlling, optical communication, and many more. This type of circuit is beneficial only when it has desirable characteristics such as low power, less delay, lesser heat generation and overheating etc. [3,15]. MUX is a digital device that transmits multiple digital data streams through a single channel on the transmitter side. Whereas on the receiver side, de-multiplexers (De-MUX) having reverse operation is fitted[2].

In this proposed paper 2-input multiplexer circuit is designed using FGMOS which is then used to construct FGMOS based 4-input multiplexer tree. After which a thorough performance analysis is done by comparing the simulation results of the above- mentioned circuits with their CMOS based multiplexer design by keeping the design parameters same.

In section 2 basics of 2-input multiplexer and 4-input multiplexer tree is covered along with the basics of FGMOS, section 3 includes LTspice simulations, section 4 includes simulation results whereas last section includes conclusion followed by references.

2 Background

2.1 2-input multiplexer circuit

2-input multiplexer accepts two data streams, then selects either of them based upon the select input code and passes it onto the output line. Multiplexer acts as a switching element by deciding which input code should be passed onto the output line. Truth table below depicts V_A and V_B are two inputs, S is select input, and V_{out} is the desired output voltage.

When S=0,output voltage is equal to V_A and when S=1,output voltage is equal toV_B.

TABLE I. TRUTH TABLE OF 2-INPUT MUX

• S	• Vout
• 0	• V_A
• 1	• V_B

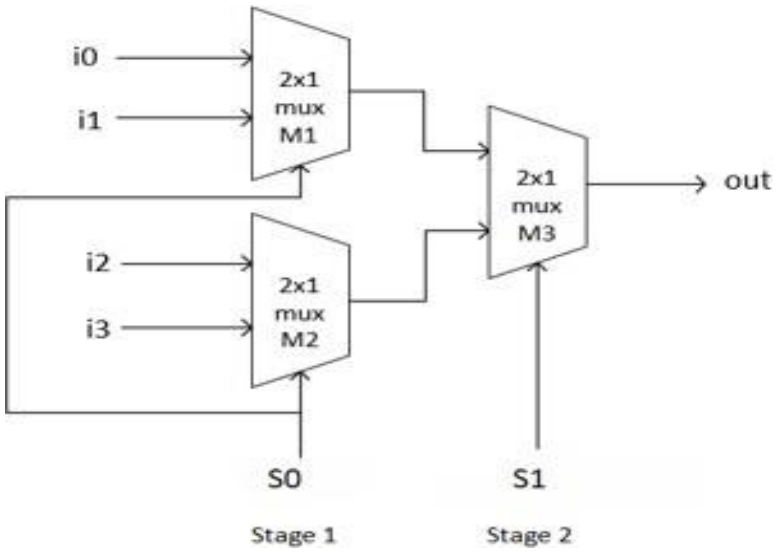

Fig. 1. 2-input mux

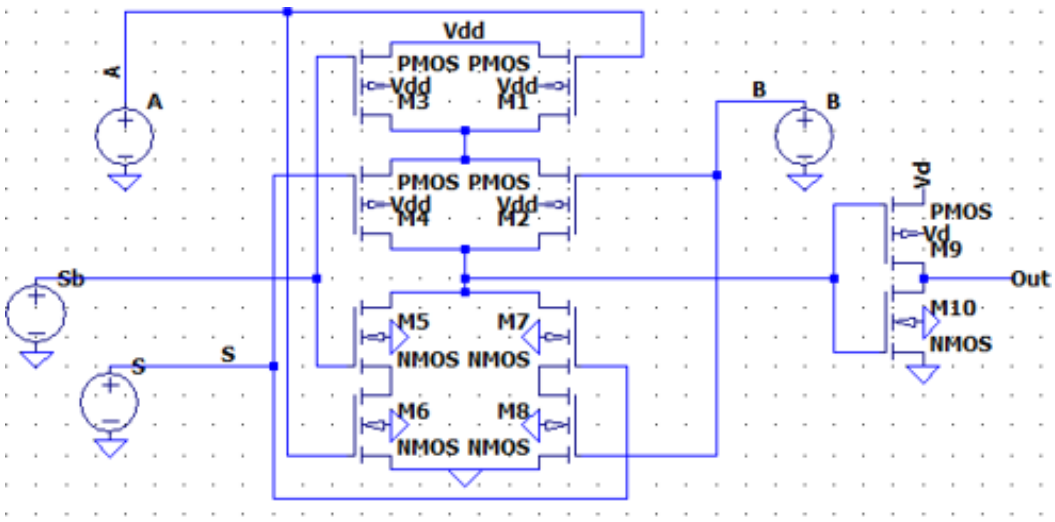

Fig. 2. 2-input mux using CMOS

2.2 4-input Multiplexer Tree

A 4-input multiplexer tree consists of three 2-input multiplexers as depicted in figure 3, it consists of two 2-input multiplexers (M1 and M2) in 1st stage having common select line S0 and 2nd stage consist of one 2-input multiplexer (M3) having select input S1. The combination of select input line decides which input is to be selected. As shown in table 2, the combination of S1 S0 will decide which input is to be fed to the

output. When S1 S0 = 00, V_A is drawn to the output line, when S1 S0 = 01, V_B is drawn to the output line, when S1S0=10,V_C is drawn to the output line, and when S1S0= 11, V_D is drawn to the output line.

TABLE II. TRUTH TABLE OF 4-INPUT MUX

• S1	• S0	• Vout
• 0	• 0	• V_A
• 0	• 1	• V_B
• 1	• 0	• V_C
• 1	• 1	• V_D

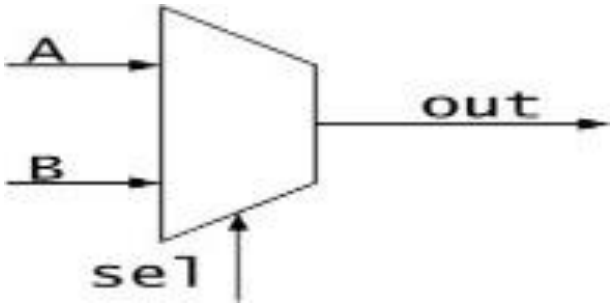

Fig. 3. 4-input mux

2.3 FGMOS technique

Floating gate mosfet(FGMOS) is a device that comprises of a normal MOS having its gate terminal surrounded by SiO_2 in such a way that the gate of the standard mosfet is electrically isolated and is then capacitively coupled to multiple controlling input gates ensuring that there exists no resistive connection to its gate [12,16]. The controlling voltage of FGMOS and the ability to add additional inputs provides the circuit with the broad range of tunability [1]. As the Floating gate is surrounded with isolating material having very high resistivity, there exists no direct connection between the gate inputs and Floating gate. Therefore, in terms of its DC operating point, the FG is a floating node [12].

FGMOS technique allows V_T adjustability without the need to reduce its feature size, thus operating at power supply voltage levels which are well below the intended operational limit. Its consumed power is also less as compared to the power required by the circuit built using normal MOS [5].

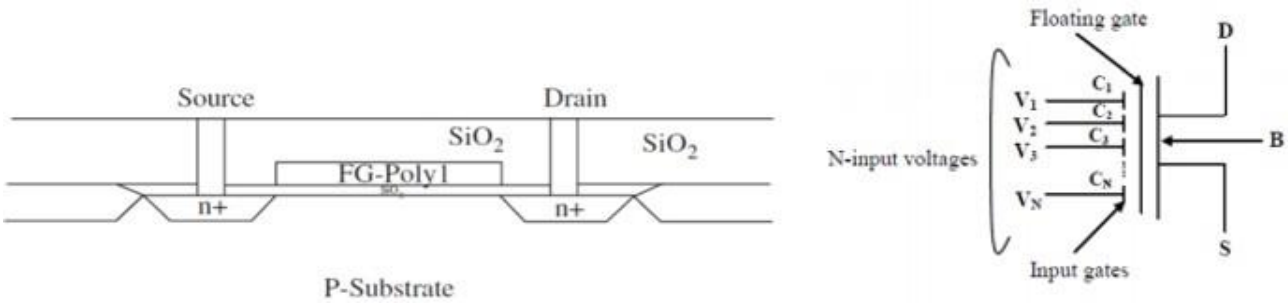

Fig. 4. Structure and symbol of FGMOS

As depicted in figure 4 the FG is surrounded by two SiO_2 insulator layers and thus electrically isolated from the rest of the device.

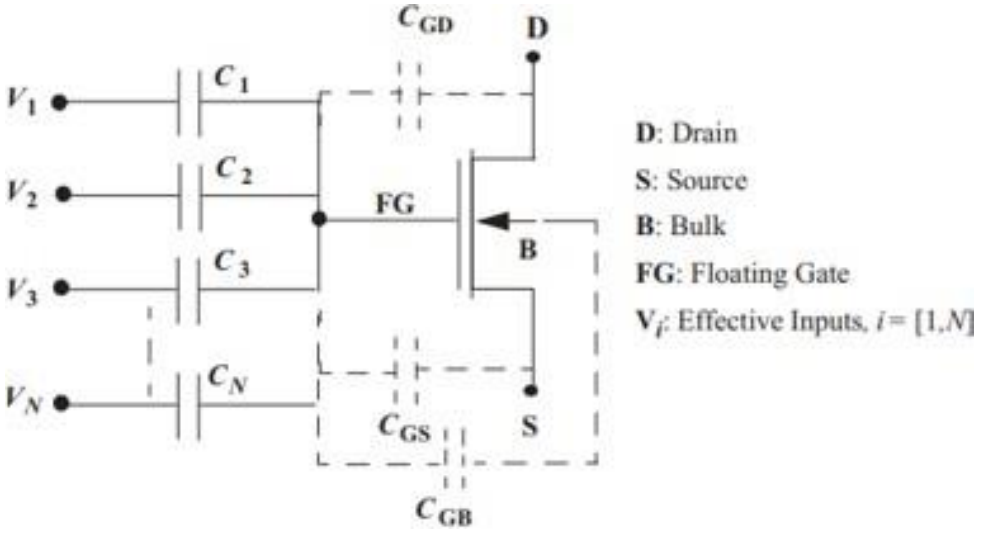

Fig. 5. Equivalent structure of FGMOS

where V_S, V_D, V_{FG}, V_n are the source, drain, floating gate and n^{th} input control gate voltage, respectively. C_n is the value of capacitance added between the n^{th} gate input (also known as control input) and the floating gate. C_{GS} and C_{GD} are floating capacitances between gate-source and gate-drain respectively. The value of the capacitance between FGMOS input and FG is determined by doing proper sizing of the input electrode which can be varied in the design stage itself in accordance with the requirement. Once the circuit is designed using a particular value of capacitor it cannot be reprogrammed in any other stage, therefore it is a very crucial step for the designer to decide the capacitor value in the beginning [12].

According to charge conservation equation applied at the floating node:

$$C_1(V_1 + V_{FG}) + C_2(V_2 + V_{FG}) — C_{GS}(V_{FG} - V_S) — C_{GD}(V_{FD} - V_D) = Q_F \quad (1)$$

where the residual charge is represented by Q_F that might get trapped inside the floating node of FGMOS during the manufacturing stage [16]. Assuming infinite value resistance between the floating node (FG) and the layers surrounding it i.e., floating node is perfectly isolated having no leakage current and making charge in the floating gate(Q_f)equal to 0 for simplicity therefore, writing the above equation as:

$$V_{FG} = w_1V_1 + w_2V_2 + w_{GS}V_S + w_{GD}V \quad (2)$$

Where w_n is the capacitive coupling ratio, defined as:

$$w_n = \frac{C_n}{C_1+C_2+C_{GS}+C_{GD}} \quad (3)$$

Equations modeling the operation of the FGMOS can be derived, in a very easy way, from the equations that describe the operation of the MOS transistor used to build the FGMOS. The characteristic attribute of the FGMOS device is the group of extra input capacitors (Ci where i = [1, N]) added between the control inputs and the floating node. C_{GD} and C_{GS} are the gate-drain and gate-source parasitic capacitance which is same for the MOS transistor fabricated using similar technology node having same active area. It is also observed that there is no effect of parasitic capacitors in FGMOS on the relationship that exists between DC I_{DS} and floating node voltage. However, these parasitic capacitors do affect the relationship that exist between floating gate voltage (V_{FG}) and control input gate voltage (V_i).

The drain current of FGMOS having two input gates in the saturation region is defined as:

$$I_D = \beta[w_1(V_1 - V_S) + w_2(V_2 - V_S) - V_{TH}]^2 \quad (4)$$

where $\beta = (\mu_n C_{ox})/2\ W/L$ is transconductance parameter, μ_n is electron mobility, C_{ox} is oxide capacitance per unit area, W/L is the aspect ratio of transistor, w_1 and w_2 are input capacitive coupling ratios, V_S and V_{TH} are source voltage and threshold voltage respectively. In this paper, one of the control gates is used for biasing (to fix threshold voltage) and the other one is used as input.

V_{TH} of the FGMOS can be tuned externally as depicted below:

$$V_{TH} = V_{T0} - \frac{\frac{C_2}{C_1}}{1+\frac{C_2}{C_1}}(V_2 + V_{DSat}) \quad (5)$$

where V_{T0} and V_{DSat} is the threshold voltage having zero bias value and the drain-source voltage of the FGMOS in saturation region respectively [6]. Equation 5 depicts that asthe voltage applied to control input gate 2(V_2) also known as bias voltage (V_b) is varied, V_{TH} of the FGMOS can be easily tuned. By effectively varying the bias voltage (V_b) it is possible to negate the sign of V_{TH} or make it zero. This tunability feature of V_{TH} in the FGMOS makes it ideal for implementing the circuit at very low voltage as compared to same circuit being implemented using normal MOS[17,18].

3 LTspice Simulation

Simulations are carried out using LTSPICE for TSMC 180nm technology for which equivalent circuit has been used in this paper and bias voltage (Vb) of 600mv has been applied along with the gate voltage (Vg) of 1V by placing capacitor and resistor in parallel between the above-mentioned external voltage node and the floating node. Values of the capacitor has been selected in femto farad range whereas resistances used are in the range of Mega Ohms. As SPICE do not accept floating node having no DC branch to ground, one resistor having very high value is added in parallel to each capacitor so that loading effect to the circuit is minimized. Each branch has equal time constant i.e., product of R and C is kept same i.e., $R_{G1}C_{G1} = R_{G2}C_{G2} = \ldots = R_{Gn}C_{Gn} = R_{FGB}C_{FGB} = R_{FGS}C_{FGS} = R_{FGD}C_{FGD}$ [4,13-15].

As depicted in equation 6 Average Power consumed (P) and propagation delay(t_p) for each circuit is calculated, which when multiplied gives PDP (power delay product). Further multiplication of t_p with PDP gives EDP where EDP is the power consumed to effectively drive the output to 90 % of its final value multiplied with the propagation delay squared.

$$EDP = PDP * t_p = Iavg * V\,dd * t_p * t_p = P * t_p^2 \quad (6)$$

V_{dd} and I_{avg} is the supply voltage and average switching current respectively [3].

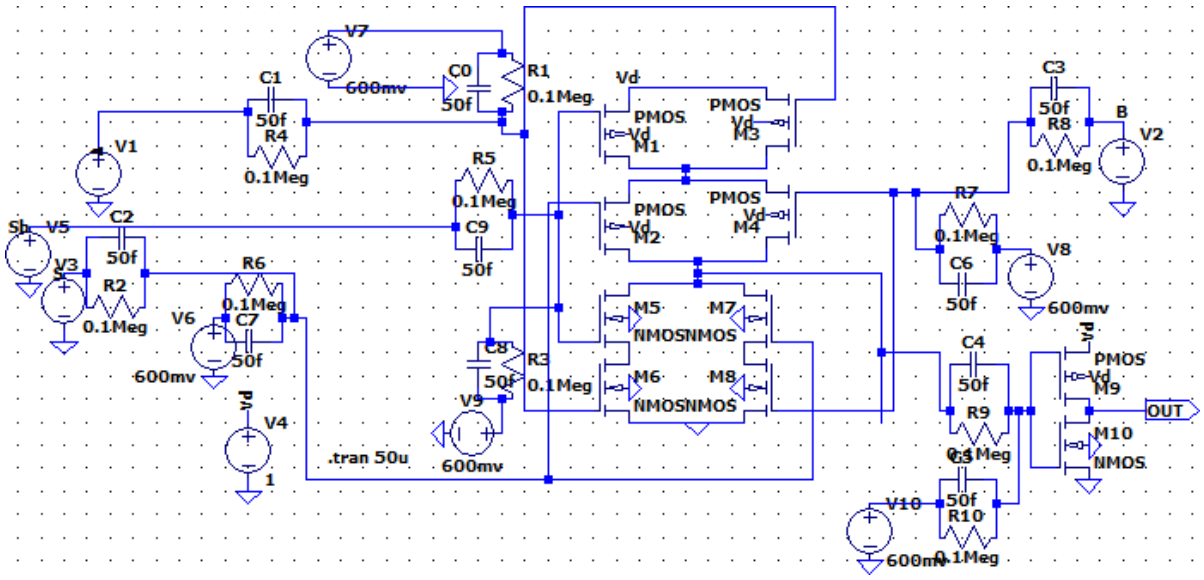

Fig. 6. 2-input mux using FGMOS

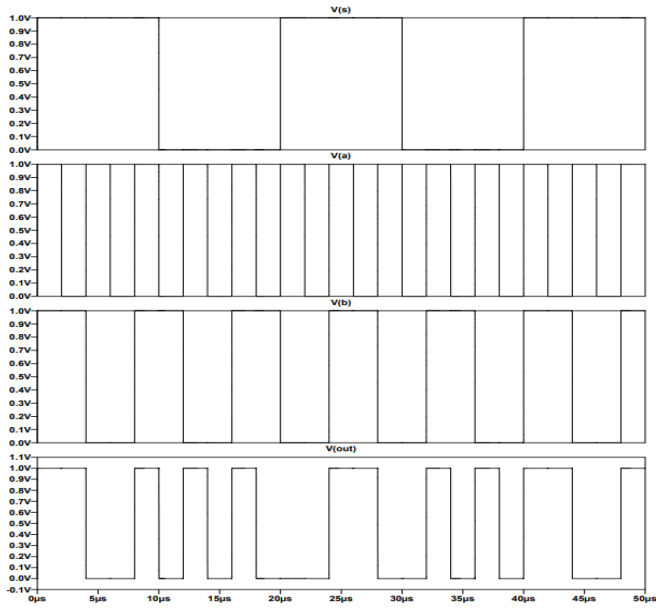

Fig. 7. Output waveform of 2-input mux using FGMOS

4 Simulation Results

4.1 Simulation Specification

Simulation of 2-input multiplexer and 4-input multiplexer tree using FGMOS is carried out by maintaining voltage supply of 1V and W/L ratio equals to 1u/0.18u for P-type FGMOS and 0.46u/0.18u for N-type FGMOS, which is then compared with the conventional cmos based multiplexer circuit. The simulation is done on LTsipce using 180 nm technology. Tool used: LTspice XVII Technology file: TSMC 180nm Technology level: 49

Power supply: 1 V

Bias:600mV

R, C: 0.1 Mega Ohm, 50 fF respectively.

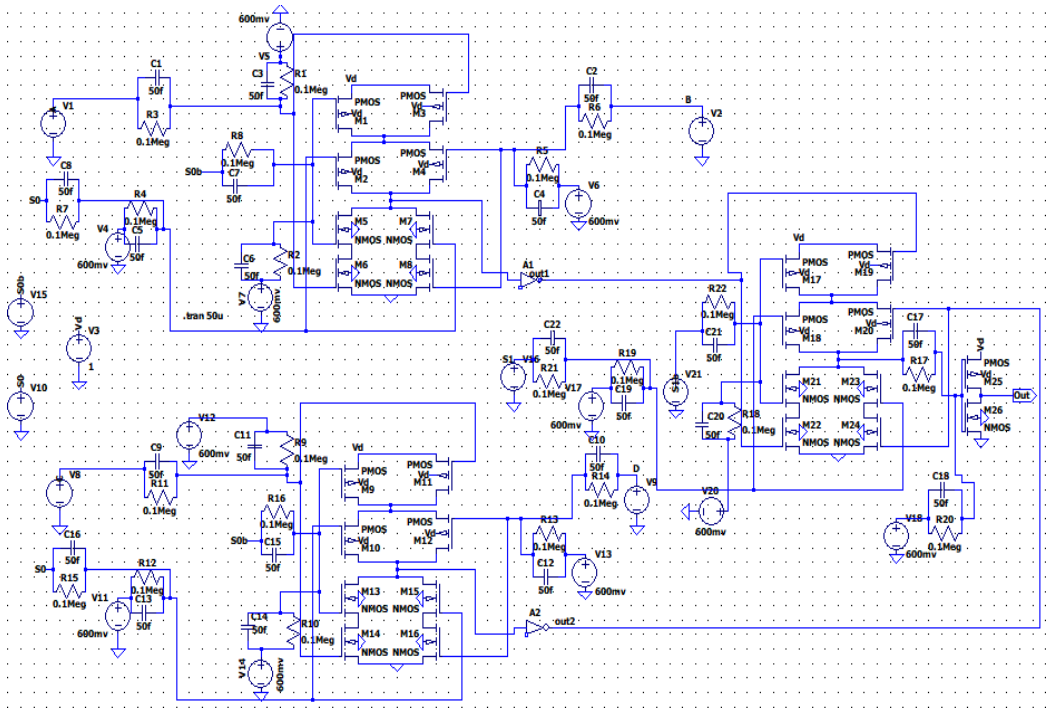

Fig. 8. 4-input mux using FGMOS

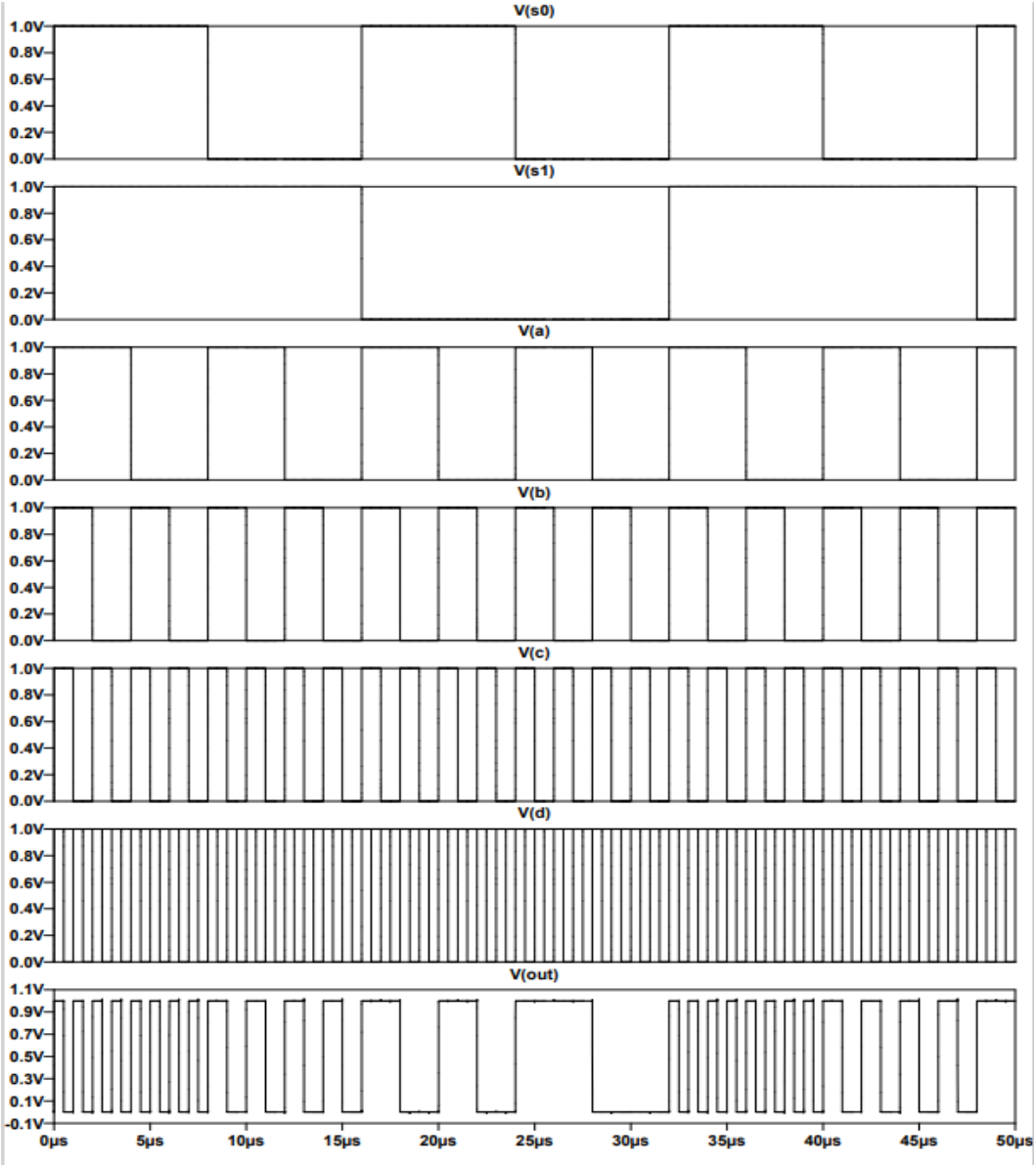

Fig. 9. Output waveform of 4-input mux using FGMOS

4.2 PerformanceAnalysis

As per the discussion carried out and the simulation results obtained, it is evident from Table 3 that the design of 2-input multiplexer using FGMOS has ultra-low power consumption i.e. 84 % less power consumption as compared to 2-input multiplexer using CMOS technique whereas 4-input mux tree using FGMOS has 70 % less power consumption as compared to 4-input mux using CMOS which in turn will lead to less overheating in FGMOS based mux circuitry. Delay of these FGMOS based circuitries is found to be decreasing with the increasing order of mux which in turn leads to less PDP in FGMOS based mux circuit.

It is clear from the analysis that as the order of mux using CMOS is increased, the delay is increasing. On the contrary, mux using FGMOS when compared to its lower order counterpart have less delay. Also, 2-input mux using FGMOS have 68 % less PDP and almost equivalent EDP when compared to mux designed using CMOS. Whereas, with the increasing order of mux EDP was much more prominent in FGMOS based mux. Therefore, design of the multiplexer using FGMOS is much more advantageous as compared to CMOS technique with increasing order.

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TABLE III. COMPARISON TABLE

• **Basis of** • **Comparison**	• **2-input** • **multiplexer**		• **4-input** • **multiplexer**	
	• ***using*** • ***CMOS***	• ***using*** • ***FGMOS***	• ***Using*** • ***CMOS***	• ***using*** • ***FGMOS***
• Power	• $938pW$	• $149.84pW$	• $4.2nW$	• $1.24nW$
• Delay(ns)	• 0.717	• 1.71	• 0.952	• 1
• PDP (nJ)	• 0.673	• 0.256	• 3.99	• 1.24
• EDP	• 0.482	• 0.438	• 3.806	• 1.24

5 Conclusion

This paper provides In-depth performance analysis of 2- input multiplexer and 4-input multiplexer designed using FGMOS and its comparison is drawn with the CMOS based multiplexer circuitry. Analysis of the behavior and performance of circuits is done using TSMC 180nm technology in SPICE. Therefore, the paper concludes with enhanced performance characteristics which includes ultra-low power consumption, low voltage power supply, less delay, improved PDP and EDP with increasing order of FGMOS based mux. Thus, FGMOS technique can be used to design mux, as with increasing order it offers better characteristics. These improved performance characteristics can be utilized in battery operated systems, modern portable electronic devices, optical communication, FPGA, biomedical equipment etc.

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