Design of Reed-Solomon Encoder for Error Detection in DRAM Cells

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Abstract

This paper investigates the design of Reed Solomon (RS) encoder. Based on the message symbols, the RS encoder generates the code-word. By carrying out a polynomial division using Galois Field algebra, the parity symbols are calculated. Reed-Solomon codes are one of the most effective and effective non-binary error codes to detect and correct burst errors. This is the focus work for my dissertation to implement RS encoder and decoder that is a complex algorithm and it is used for the reliable memory operation in a system. The RS Encoder and decoder are design in structural modeling and develop the hardware. The sift and multiplier type divider is used for Encoder and Syndrome module design.

Keywords: Reed-solomon codes, Galois field, DRAM memory, VHDL, Synthesis

1 Introduction

The constant scaling down in CMOS technologies added to reduction on the levels of power supplies are making the circuits much more sensitive to noise. When high reliability is needed, techniques must be used to deal with this problem. As in the case of human-involved, military or space application, the fault tolerance becomes a major concern. When a highly energized particle impinges the silicon, electron-hole pairs are created producing transient current pulses that alter normal operation of a system. This problem used to be more frequent in space applications, but today even at sea level is becoming important. This is because of the shrinking of the device size and the minimum charge, named critical, needed to charge or discharge parasitic capacitances. In the case of memories, at less two types of errors could occur. The first one of them is an alteration of the data stored in the array. This problem occurs when the particle hits the nodes where transistors are off, that are the sensitive places of the cell, producing a flip on the bit stored. Normally this is referred as a single event upset (SEU). The second problem affects combinational logic and sense amplifiers that are used in the periphery of the array to store and read data. If highly enough, a single event transient (SET), could be propagated as a signal through the gates, or produce a wrong write or read process. Coping with the first problem error detection and correction codes (EDAC) have proven to be very effectives.

Error Correction Code (ECC), Hamming Code (SECDED), Single Error Correction and Double Error Detection is widely used to detect and correct soft errors in the memory of caches. ECC retains the check bits per data unit. The all the one-bit error detecting and the correcting code are not sufficient for large word memory because in large word case error may come in Multi Bit so Multi Bit error correcting algorithm are needed. The Cyclic code is used in Multi bit error correction. It is used in communication and the storing device for error detecting and correcting. The Reed Solomon also used for Multi Bit error correction, but it is full mathematical algorithm and very complex [1,2].

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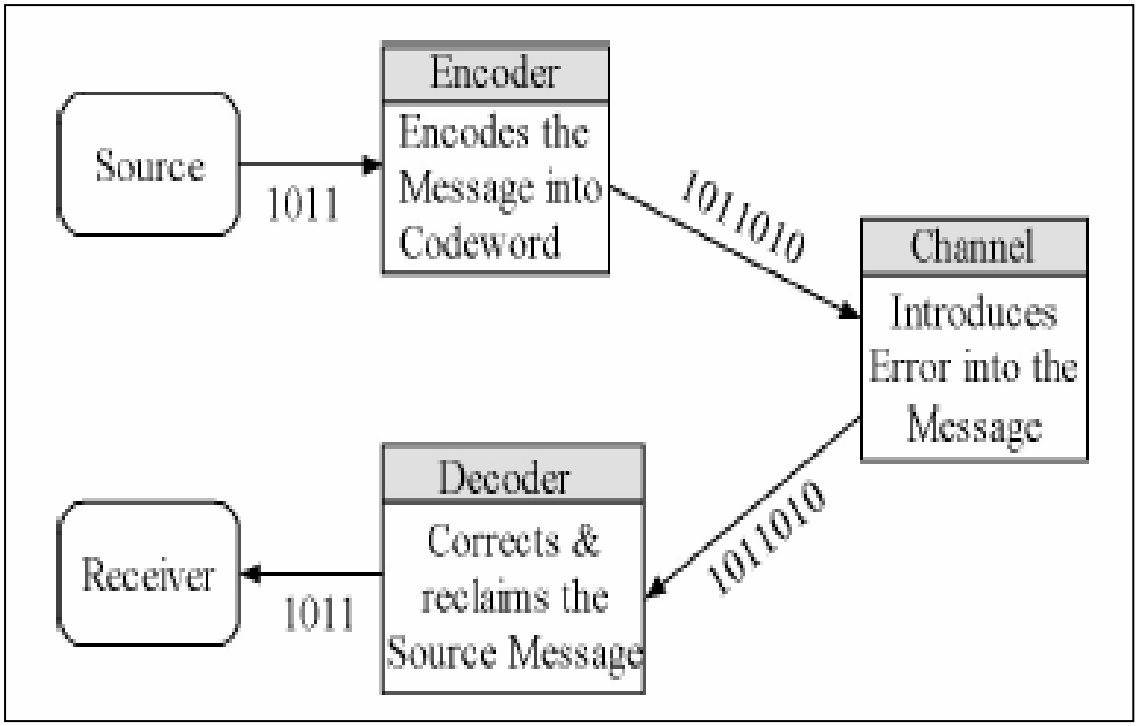

Fig.1. Reed-Solomon Encoder-Decoder

The RS encoder given at the end of the transmitter encodes the input message and transmits it through the channel into a codeword. Noise and other channel disturbances can interrupt the codeword and corrupt it. This corrupted codeword reaches the end of the receiver (decoder), where it gets checked and the receiver receives a corrected message. A decoding failure may occur if the channel-induced error is greater than the error-correcting capability of the decoder. If a codeword is passed unchanged, decoding failures are said to have occurred, a decoding failure would result in an incorrect message being sent to the output. While listed as non-binary in the definition, it is also possible to operate RS Codes on binary data.

2 Error Detection and Correction

If a codeword is passed unchanged, decoding failures are said to have occurred, a decoding failure will result in an incorrect message being sent to the output. While listed as non-binary in the definition, it is also possible to operate RS Codes on binary data The reverse is also true; if the channel offers a certain possible transmission rate, ARQ allows a higher information rate than FEC, especially if the channel has a low error rate. FEC, though, has the advantage that a response channel is not needed. In each case, however, the option depends on the properties of the device or the application in which the error-correction should be applied. In many applications, such as radio broadcasting or Compact Disc, there is no answer channel (CD). Another advantage of the FEC is that the transmission is never completely blocked, even if the channel output falls to such low levels that the ARQ system would have needed retransmission entirely. The receiver has no real-time communication with the transmitter in a device that uses FEC and does not check whether the data has been received correctly. To either repair it or announce an alert, it must decide on the data obtained and do whatever it can. The implementation of Error-Correcting Coding is based on two key approaches. The stream of symbols in one of these is split into blocks and coded. It is therefore referred to as Block Coding. A convolution operation is added to the symbol stream in the other one. This is Convolutional Coding called. [3,4].

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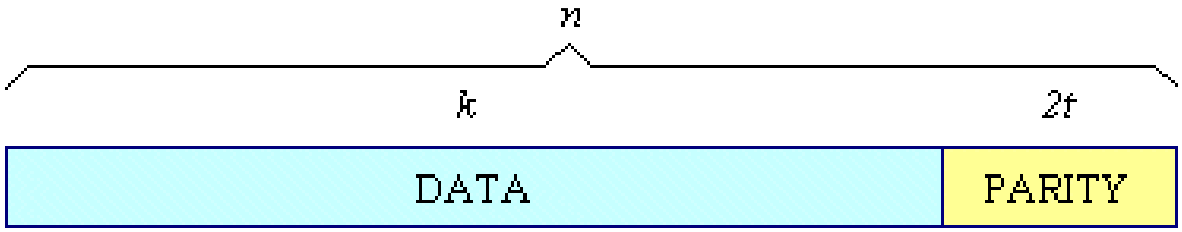

Fig.2. Reed-Solomon Code

3 Reed Solomon Codes

The family known as block codes belongs to RS codes. This family is so called since a block of message symbols is interpreted by the encoder and then outputs a block of code-word symbols. RS codes, to be exact, are non-binary systematic cyclic linear block codes. With symbols that consist of several bits, non-binary codes function. 8 bits, or a byte, is a typical symbol size for non-binary codes. Non-binary codes such as RS are efficient at correcting burst errors as the correction of these codes is done at the symbol level. By interacting with symbols in the decoding process, these codes can correct a symbol with a burst of eight errors, just as easily as they can correct a symbol with a single-bit error. A systematic code produces codewords in unaltered form containing the message symbols [5,6]. The encoder applies a reversible mathematical function to the symbols of the message to produce symbols of redundancy, or parity. By appending the parity symbols to the message symbols, the codeword is then created. When it is systematic, the implementation of a code is simplified.

A code is cyclic if another valid codeword is also generated by a circular change of some valid codeword. Due to the existence of effective decoding techniques for them, cyclic codes are common. Finally, a code is linear if the addition of any two valid codewords results in a single valid codeword as well. RS codes with m-bit symbols are usually expressed as an RS(n, k), where.

Block Length	n
No. of Original Message symbols	k
Number of Parity Digits	n - k = 2t
Minimum Distance	d = 2t + 1

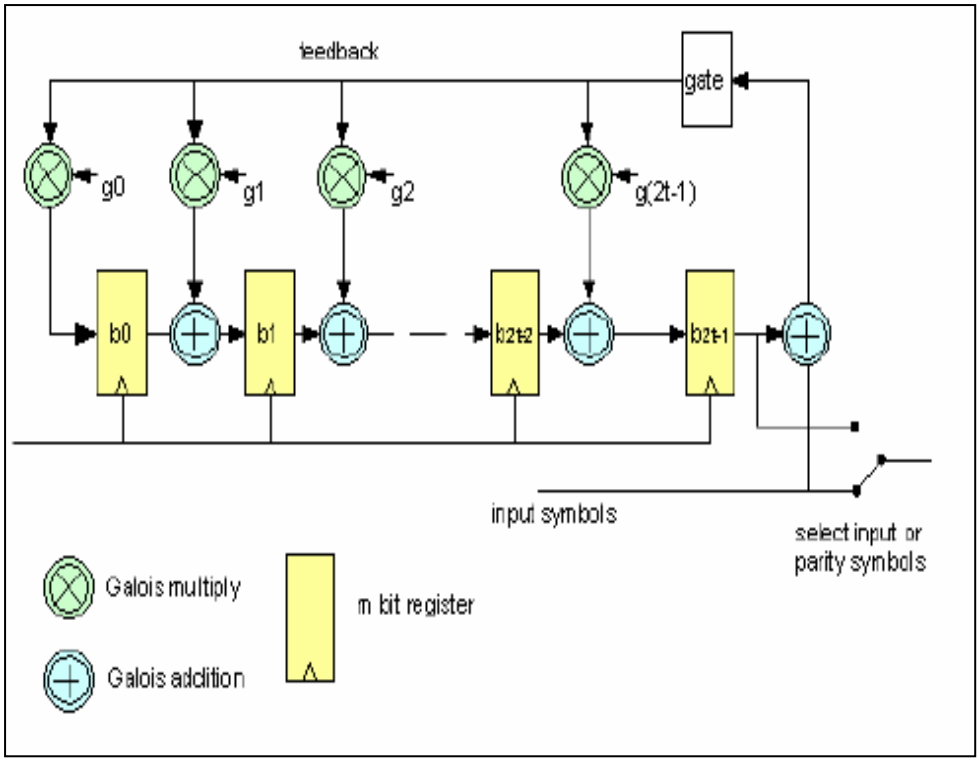

Fig.3. Reed-Solomon Encoder Architecture

TABLE I. DEVICE PARAMETER

Target FPGA Device	Vertex 2 Pro
Word Size(n)	155bit
Data word size(k)	105bit
Parity Size(p)	50bit
Packet(block)	5bit
Hardware description language	HDL VHDL
Tool	Xilinx ISE 7.1i and ModelSim SE 5.7f

4 Results and Discussion

Reed-Solomon (RS) codes have many applications for communication and memory and are very effective in dealing with burst errors, especially when two RS codes are 'interleaved' for error control. The burst error channel is efficiently converted, using interleaving, into an independent error channel for which several FEC coding techniques are applicable. Therefore, the combination of interleaving and FEC provides an efficient way to counteract the effect of error bursts. In this project, a (31, 21) RS code has been implemented in VHDL. The encoding and decoding of the (31, 21) RS code using various modules and their simulation results are given in this section.

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TABLE II. INPUTS AND OUTPUTS

SIGNALS	DIRECTION	USAGE
Reset_n	INPUT	reset function of the code
Data_in	INPUT	information bits
Data_out	OUTPUT	encoded data
Input_strobe	INPUT	when 1 data_in is valid
Output_strobe	OUTPUT	when 1 data_out is valid
Count	SIGNAL	counts the data bits upto data_size
Data_size	INPUT	no. information bits
Sum	SIGNAL	total sum of bits
Parity_register	SIGNAL	parity registers containing parity bits

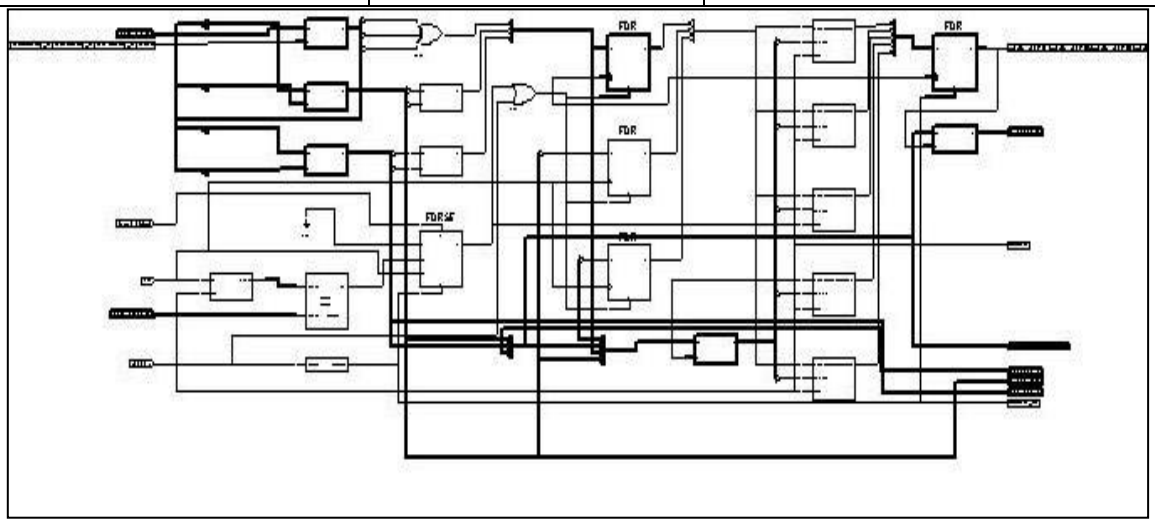

Fig.4. RTL Schematic of Reed-Solomon Encoder

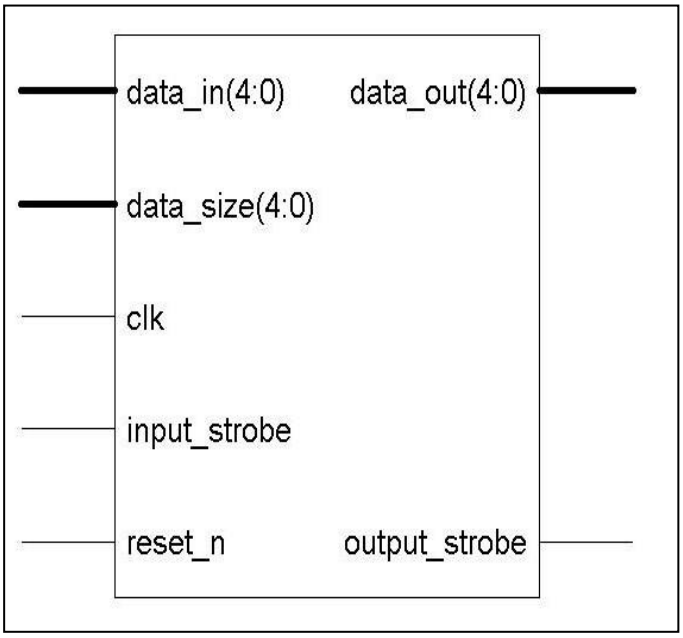

Fig.5. Schematic of Reed-Solomon Encoder

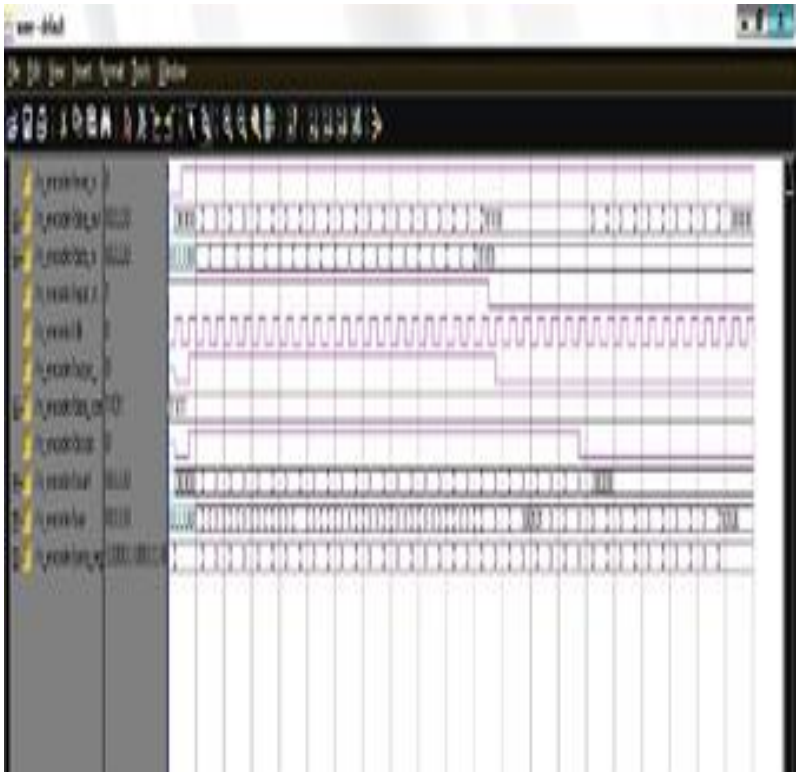

Fig.6. Waveform of Reed-Solomon Encoder

5 Conclusion and Future Scope

An implementation of reed-solomon encoder for error detection in DRAM memory cell is carried out. The encoder splits the incoming data stream into blocks by adding redundancy according to a specified algorithm and processes each block independently. The symbols used are the elements of a finite Galois field in the block codes. Due to modulo arithmetic followed in the finite fields, the product of any algebraic operation is mapped into the field and thus rounding problems are conveniently solved. So adding, subtracting, multiplying or separating two codewords is a true codeword within the field again. All encoded data symbols are Galois field elements that are defined by the application parameters and properties of the system. The encoder is implemented with feedback using linear shift registers. For implementation of Reed Solomon in memories a decoder is to be designed which could effectively detect and correct error in the information bits.

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