Design and Analysis of a Dual Material Triple Gate TFET with the Pocket Doping for the Performance Enhancement

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Abstract

In this investigated work, we have analysed the miscellaneous figure of merit for Double metal Triple gate TFET. Various techniques have been utilized to improve the ON-state driven current in the drain by doing a comprehensive analysis. Different techniques are examined and correlated by using the TCAD Silvaco tool to get excellent ON current. Further work function engineering has been done in the optimized DMTG-TFET to increase its performance and finally, we introduce pocket doping that increases the ON current (2.34×10^{-3}) and also I_{ON}/I_{OFF} ratio (4.36×10^{14}) with subthreshold (SS) of 25.8mV/decade. The pocket doped DMTG-TFET adequately suppress the ambipolarity and endeavour about 20 times higher I_{ON} as compared to conventional DMTG-TFET.

Keywords: DMTG-TFET, Broken gate, Pocket doping, Band-to-band tunnelling.

1 Introduction

In terms of increased package density, the IC industry has obtained remarkable remittance in compliance with Moore's law and backed by Dennard Scaling Theory principles [1]. As in the modern era, there are requirements of low operating power and high-speed technologies that have needed to down-scaled the feature size of the CMOS devices to Nano level dimensions[2], [3]. But the ceaseless downsizings of the feature size of the MOS device has created several short channel effects and increased the power dissipation as well as causing high leakage [4], [5]. When the device is in the OFF-state because, in short channel length devices, like any long channel devices, the gate does not have much electrostatic control [6]. As the current transport mechanism followed the charge injected into the channel over the barrier in traditional MOSFETs, so it suffers from the limits of the subthreshold swing to 60mV/decade, which restrict the scaling of the supply voltage [7], [8]. The restriction of traditional MOSFETs is repressed by adjusting the geometry of the gate, the geometry of the system, and improving the process of charge injection to match the technology change [9], [10].Gate geometry involves multiple-gate (the double and triple gate) devices that have improved options for adaptability to resolve the impediment of SCEs in Nano-scale devices [11]. The multi-gate technique, however, was unable to limit the rolling -off action of the threshold voltage in MOS devices and also had the effect of the drain biasing on the current when the MOS devices scaled-down below 20nm [12], [13]. To conquer these aforesaid problems, Tunnel FET is evaluated as the best suitable alternative for MOSFET among all new devices according to researchers[14]. Band-to-band tunnelling is the operating theory of TFETs, which helps to obtain the subthreshold swing (SS) below 60mV/decade, which is about impossible in MOS devices. This ability makes the TFET an excellent candidate for the application of low power and low voltage [15], [16]. But, TFETs also encounter some critical issues like low ON current (Ion), ambipolar conduction current, and inferior RF performances. In the past few years, a lot of research work has also been accomplished to elevate the current during the ON state in TFETs.Which includes the gate engineered TFETs for decreasing the ambipolar current. To increase the ON current Heterojunction TFET in place of conventional homojunction structure and high

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k dielectric material under the gate is used [17]. There are two ways for increasing ON current one of them is by modifying the device structure and the other is by using new materials. Without changing material arrangements, the newest geometries of devices like L-shaped channel TFETs (LTFET) [18], [19] and T-shaped channel TFETs have shown better ON current (I_{ON}). But these TFETs acutely affected by the notable ambipolar current.

In this paper, we have analyzed the dual material triple-gate (DMTG-TFET) schematic and do some optimization to suppress the ambipolar current and increase the I_{ON}/I_{OFF} current ratio. The designed device is the combination of double gate TFET (DGTFET) and L shaped channel TFET [20] with some advancement.This device elevates the ON current and provides a steeper subthreshold characteristic than the normal silicon-based broken gate TFET, LTFET [21] and DMBG-TFET [22] structure without negotiating ambipolarity of current.Finally,we use the pocket engineering approach [23], [24]near the source-channel junctionwhich enhances the I_{ON} of the device.

2 The device structure of dual metal triple-gate (DMTG-TFET)

The structure ofthe device which is taken for investigation is shown in figure 1. The 2D schematic diagram of hetero dielectric dual-material triple gate (DMTG) TFET with Sio2/Hfo2 as gate oxide is quite instinctive and has kept simple so that no issue has been inaugurated in the form of gate engineering, dielectric altering or material system. The proposed device has three pairs of the gate: three are the front gate and three are back gate. During all simulations, the gates are connected to the same external gate voltage and aluminium metal gate contacts are used. To reduce ambipolarity HfO2 near-source region and Sio2 near the drain region are chosen. Also, we kept the source doping fairly higher than the drain to suppress the ambipolarity. The tapered channel toward the drain end decreases the effective area and suppresses the probability of reverse tunnelling current that flows back from drain to source whenever the gate supply voltage is reversed. The thickness of the channel increased towards the source to decrease the effect of drain voltage in the BTB generation rate and also improve the gate controllability over the drain current, which reduces the SCEs. To reduce the reverse tunnelling current and to improve SS the thickness of the channel slim down near the drain region with a low-k dielectric as compare to the source. From Fig 1, L_{C1}, L_{C2}, L_{C3} denotes the channel length before and after optimization. $T_{SIa}$and $T_{SIb}$are the initial and tapered thickness of the substrate (the channel). T_{OXa}, T_{OXb}, T_{OXc} represents the thickness of oxide below the three gates. To represent the length of the source and drain L_S and L_D are used respectively. For exploring the prosperity of gate material engineering two distinct gate materials M1 with work function Φ_{m1}near-source side and M2 with work function Φ_{m2} near drain side as well at middle channel has been taken. The middle gate elevates the gate voltage controllability on drain current and suppresses drain voltage control on current.

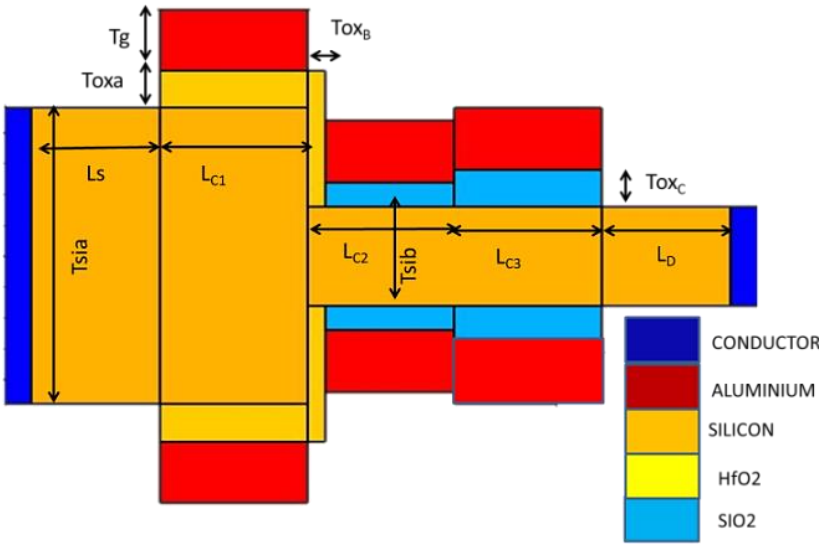

Fig.1. Schematic of the Dual material triple gate TFET

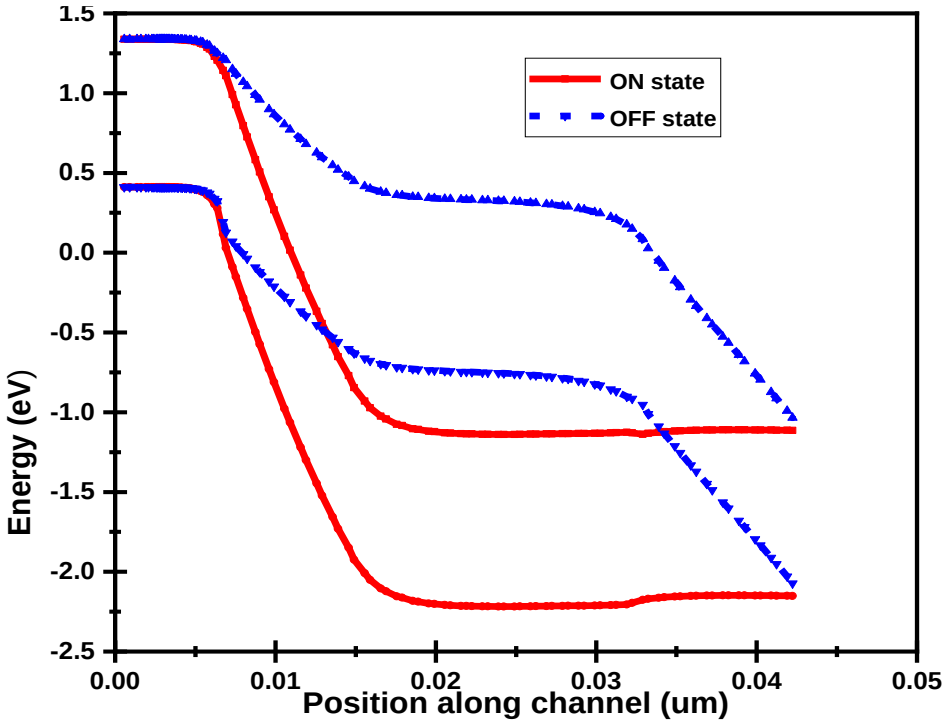

Fig. 2. Energy band Diagram of the device during ON and OFF State

3 Analysis and optimization of the Device Parameters

The Optimizations of the device were done after investigating simulated I_D versus V_{GS} plots at V_{DS}=1.2v. Optimizations were made to achieve the maximum possible on-state current, lower off-state current and enhanced subthreshold slope with the reduced ambipolar current.These objectives were inherently dependent on each other (e.g., When trying to raise the ON current It tends to raise the off-current; Similarly when trying to suppress the ambipolar current, the ON current also decreases), after observing all the changes the final device dimensions and doping value are selected by keeping the best value for all the four objectives. The plots shown in Figures.3-9 areobtained by measuring the forward ON-current at V_{GS}=1.5 V and reverse current at V_{GS}=-1.5 V. The threshold voltage is taken at a current of 10^{-8}A/um and off-state voltage at 10^{-17}A/um. The average subthreshold slope is calculated over nine decades of current from 10^{-15} to 10^{-7}A/um. From Fig it seems clear that decreased device length gives a better result in terms of ON-current, OFF-current and SS.

The optimized length of the source, drain and channel are chosen from the plot of I_D vs V_{GS}figure-3, and the final selected length of the source, drain and channel are 7nm,10nm and 26nm (i.e.,8nm,10nm,9nm) respectively [26]. It was observed that the effect of ambipolarity reduced when L_D (the drain length) kept slightly higher. In our case, the subthreshold swing increased with the proper selection of channel length as shown in Fig-5. The oxide thickness variation shown in Fig-6 approve that Thinner oxides givea better result, but the oxide thickness was kept constant at 2nm to avoid excessive gate leakage.In the table-2, theinitial and optimizedvalues of the parameter are listed. All the optimized results obtained from simulation are by no means rigid, and it is possible to choose the parameter value in such a way that one criterion over another is favored.All the simulated data are extracted from the ATLAS device simulator in the Silvaco TCAD tool. Fermi Dirac Statistics, the electric field and concentration-dependent mobility are used to show that TEFT is a high doping device. Shockley Read Hall recombination and Auger recombination model, nonlocal BTBT models have been activated along with a bandgap narrowing model during simulation of device. In Figure 9, the $I_D$vs V_{GS} (transfer-Characteristics of old and optimized devices)

are compared and the result shows minimal ambipolarity and maximal drain current in this proposed device after optimization. In our simulation dynamic, for parameter optimization, a nonlocal tunnelling model was used without any quantum correction. From some research paper, it is approved that quantum correction models which used in our model are partially coupled with the band-to-band tunnelling model. So results might somewhat vary in reality.

ID versus VGS transfer characteristics for variant lengths of the device has been shown in the figure-3.

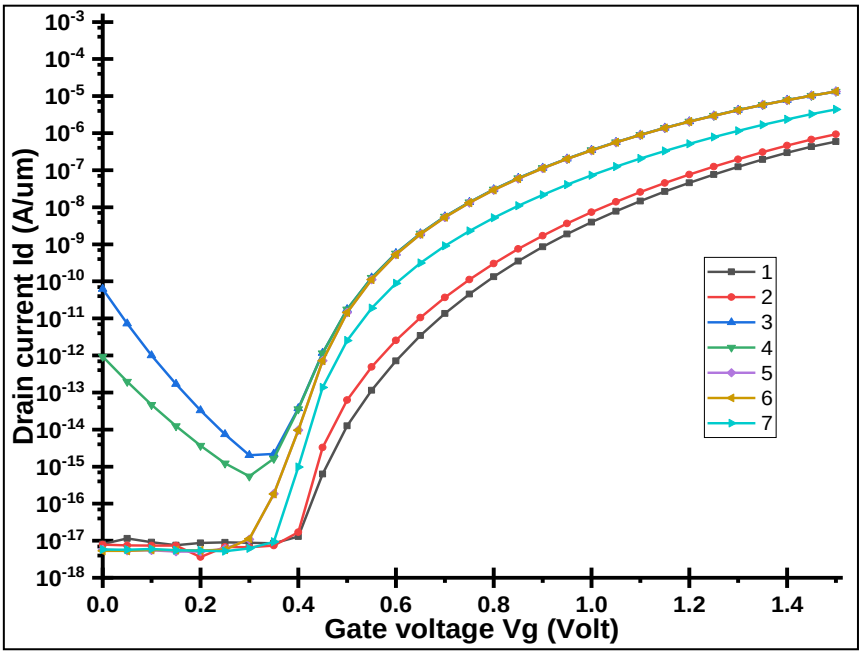

Fig. 3. ID versus VGS characteristics for different sizes of the device. To understand the graphs follow the table 1

TABLE 1. DIFFERENT SIZE OF STRUCTURE AND CORRESPONDING NUMBERS

Symbols in graph	L_S (nm)	L_{c1} (nm)	L_{c2} (nm)	L_{c3} (nm)	L_D (nm)
1	14	16	16	16	14
2	12	14	14	14	12
3	8	8	8	8	8
4	8	8	8	8	10
5	8	8	10	8	10
6	7	8	10	8	10
7	10	10	10	10	10

There was an ambipolarity effect when device size is taken as 3 and 4 (from table 1) due to channel-to-drain tunnelling. To suppress this effect the drain length must be increased so that the tunnelling distance from the channel valence band to the drain conduction band increased. From the above I_D versus V_{GS} transfer characteristics, it has become very easy to select the device size. At symbol number 6 the drain current has the highest amplitude with subthreshold slop below 30mv/decade which implies; at that device length the drain current elevated and also the device has a reduced effect of ambipolarity. In the graph, it can be seen that if the drain length selected below 10nm then the ambipolarity effect exists in the device.At device size 7, when we increase the device size near to source-channel region, the gate control over the source region

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decreased so the I_{ON} also reduced (As tunneling probability is directly proportional to tunnel path).The proposed device also shows an improved I_{ON} /I_{OFF} ratio in figure 4.

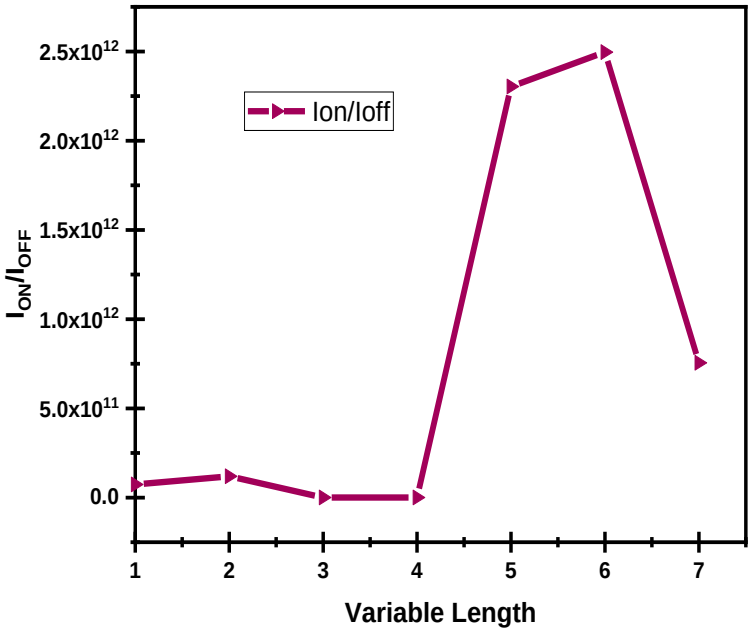

Fig.4. ION / IOFF versus the different size of length where x-coordinate represents table 1 values

Figure 5 demonstrates the effect of device length variation on the subthreshold slope. The proposed device after optimization has a better subthreshold slope (less than 30mV/decade) as shown in figure 5 which will allow this device for low power digital applications.

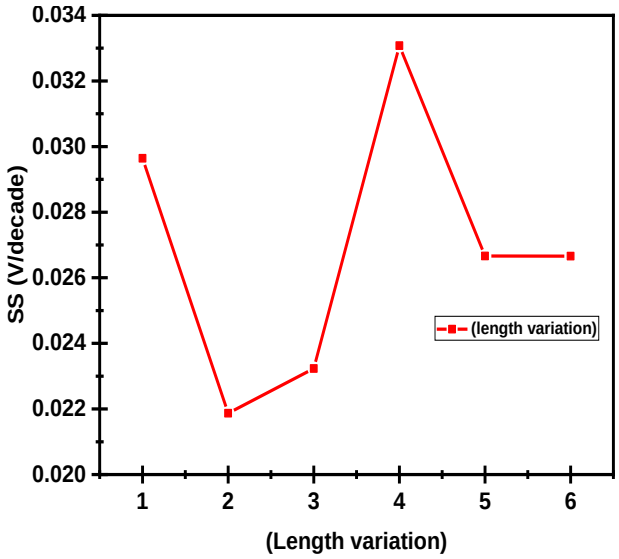

Fig.5. Sub threshold slope versus the different size of length where x-coordinate represents table 1 values

4 Oxide thickness variation

Gate oxide thickness variation is an important scaling factor because by proper scaling of gate oxide thickness one can easily increase the ON-state current and reduce the short channel effects. Commonly, in almost all TFET device structures, uniform oxide thickness is used along the channel. In this paper, a nonuniform gate oxide has been taken and the corresponding I_D versus V_{GS} characteristic shown in figure 6. From the figure, the above-stated statement verified that the ON current has improved with lower leakage current and reduced ambipolarity.

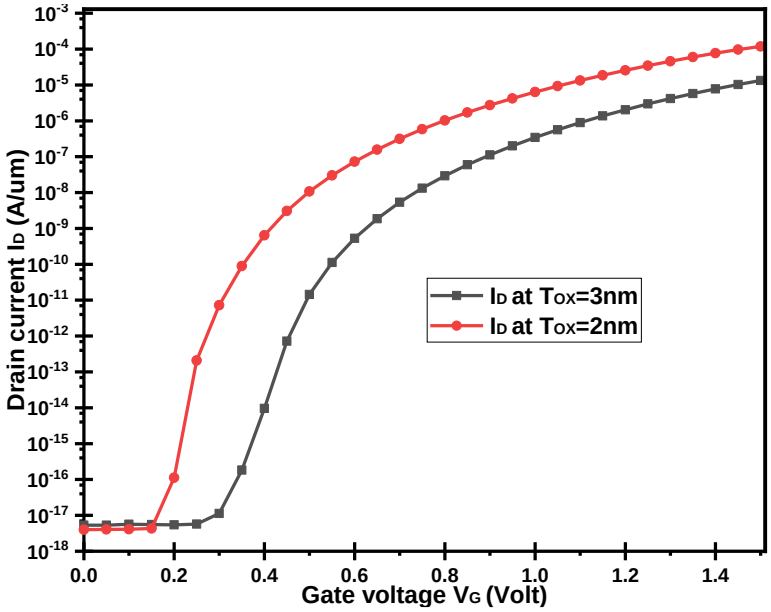

Fig.6. ID vs VGS for TOX=3nm and TOX=2nm after doing length optimization

TABLE II. DEVICE PARAMETERS BEFORE AND AFTER OPTIMIZATION

Parameters	**Initial values**	**Final values**
Channel length L_{C1},L_{C2},L_{C3}	16nm,16nm,16nm	8nm,10nm,8nm
The thickness of device Tsi_a,Tsi_b	24nm,8nm	21nm,7nm
Thickness of oxide Tox_a,tox_b,tox_c	3nm,2nm,3nm	2nm,1nm,2nm
Source length (L_s)	14nm	7nm
Drain Length (L_d)	14nm	10nm
Source Doping Conc. (N_S)	$10^{20}/cm^3$	$5\times10^{20}/cm^3$
Drain Doping Conc. (N_D)	$10^{19}/cm^3$	$1\times10^{18}/cm^3$
Channel Doping Conc. (N_C)	$10^{18}/cm^3$	$1\times10^{16}/cm^3$

5 Work function selection

The work function of the gate electrode has selected by doing work function engineering. Figure7shows the I_D VS V_{GS} plot for a different work function of the gate electrode (near-drain end). We try to keep lower work function near-source end as compare to drain end because it has directly contributed an optimal level of tunnelling and hence improves the threshold voltage as well as ON-current of device [27]. A detailed comparison of absolute electric field variation along with the channel length of the proposed DMTG-TFET with the previous device has been presented.And the outcome of that study indicates that there is a higher peak overshoot across the source side at the same gate and drain voltage, which means an increased probability of tunnelling near the source-channel junction.

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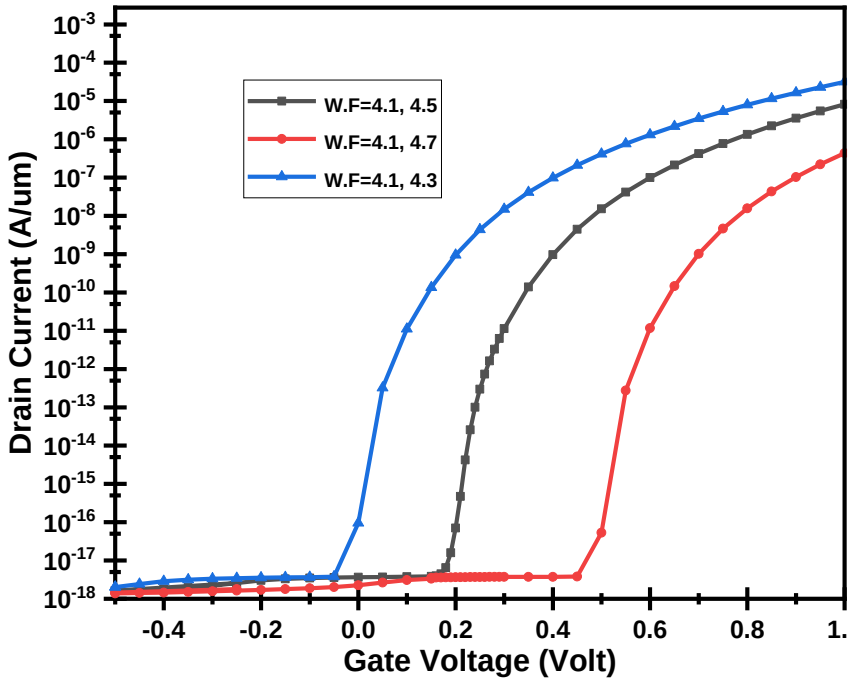

Fig.7. Drain Current Vs Gate Voltage for different work function at the drain end gate electrode

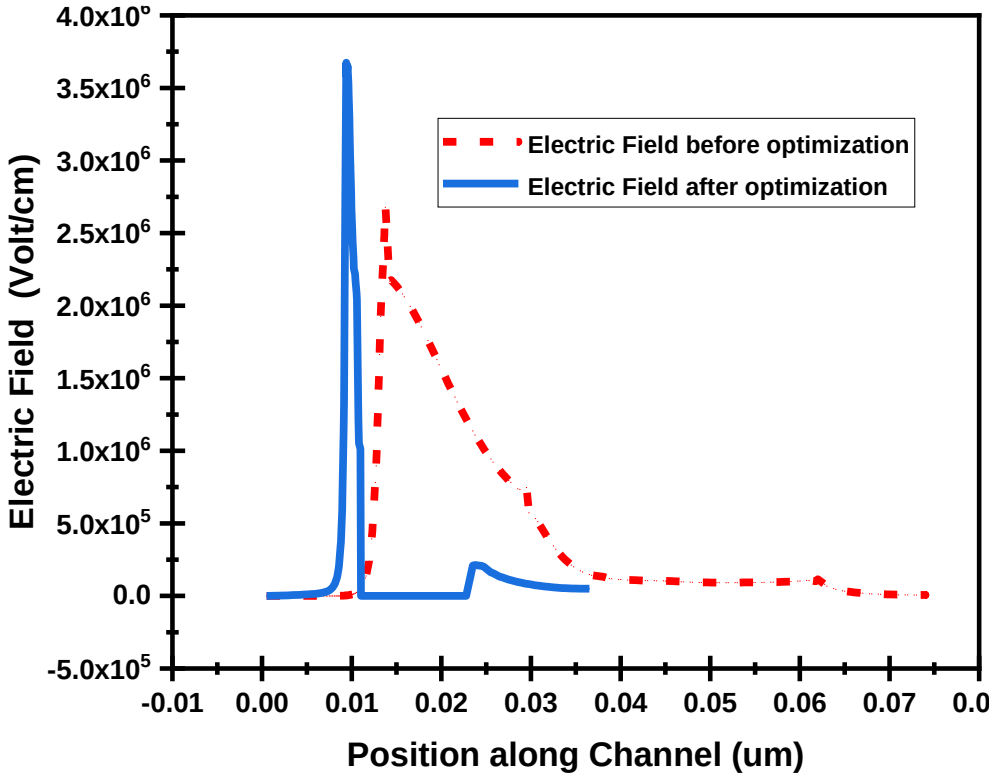

Fig.8: Electric Field Variation of old (dotted line) and optimized (solid line) device along channel

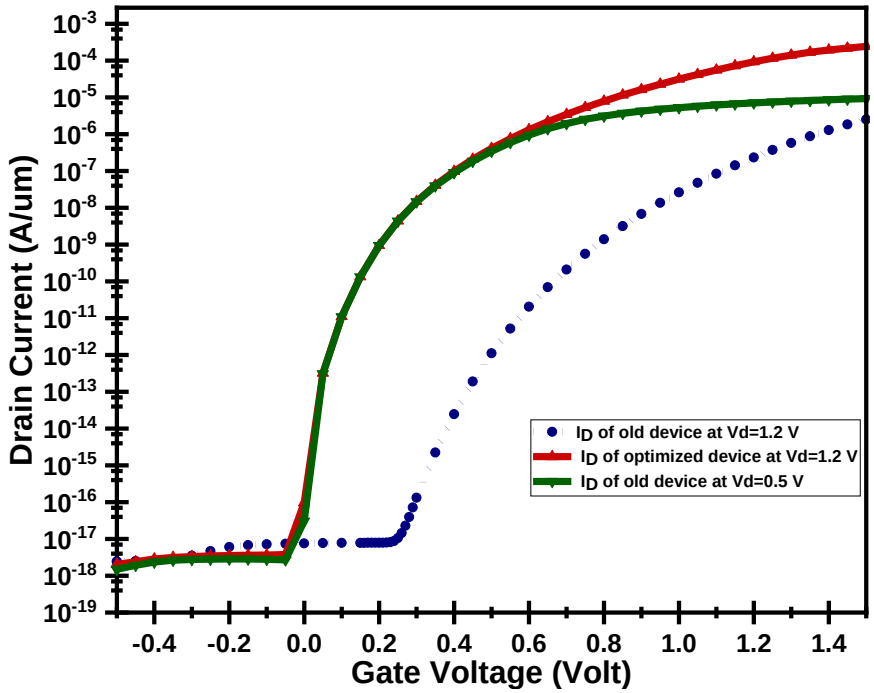

Fig.9. ID Vs VGS of final optimized device and the old one at Drain Voltage VDS=1.2, 0.5 solid lines are for the optimized device and dotted lines are for the conventional device

By doing proper modelling of TFET *I-V* characteristics, we have found that an increased ON current, reduce OFF current as well as ambipolar effect and also reduce SS as shown in figure 9.

6 Dual Metal Triple-Gate (DMTG-TFET) with the Pocket Doping

Furthermore changing the doping concentration of the drain region, adding pockets and delta doping at the source-channel junction helps to reduce ambipolarity and improve ON current. After doing all the modelling (as stated above), we have triedthe pocket doping technique so that we reduce the threshold voltage device and further increase the ON current as well as improvement in SS.A pocket has introduced at the source-channel junction having P+ type doping with the concentration of $10^{19}/cm^3$ shown in figure 10. Introductions of the pocket enhance the tunnelling at the source-channel junction.

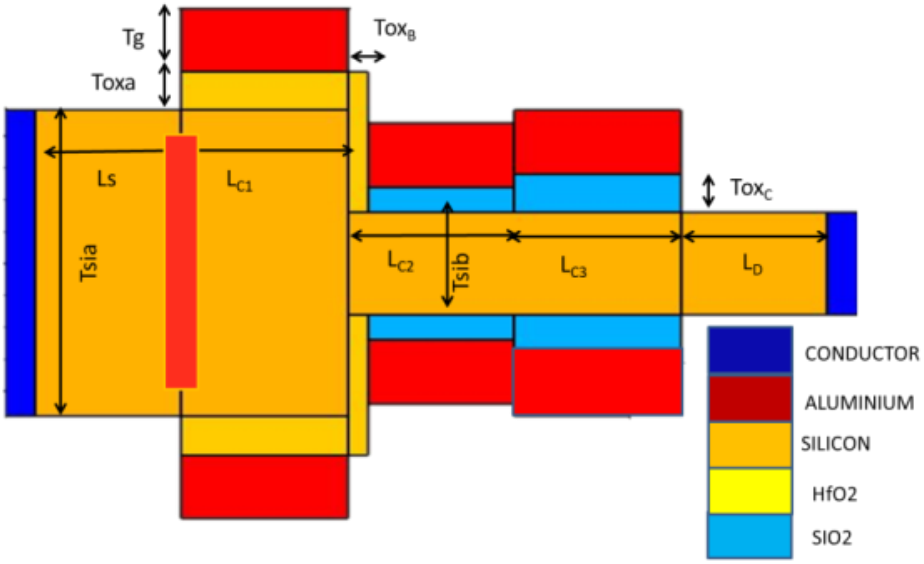

Fig. 108.Schematic view of the pocket engineered DMTG-TFET

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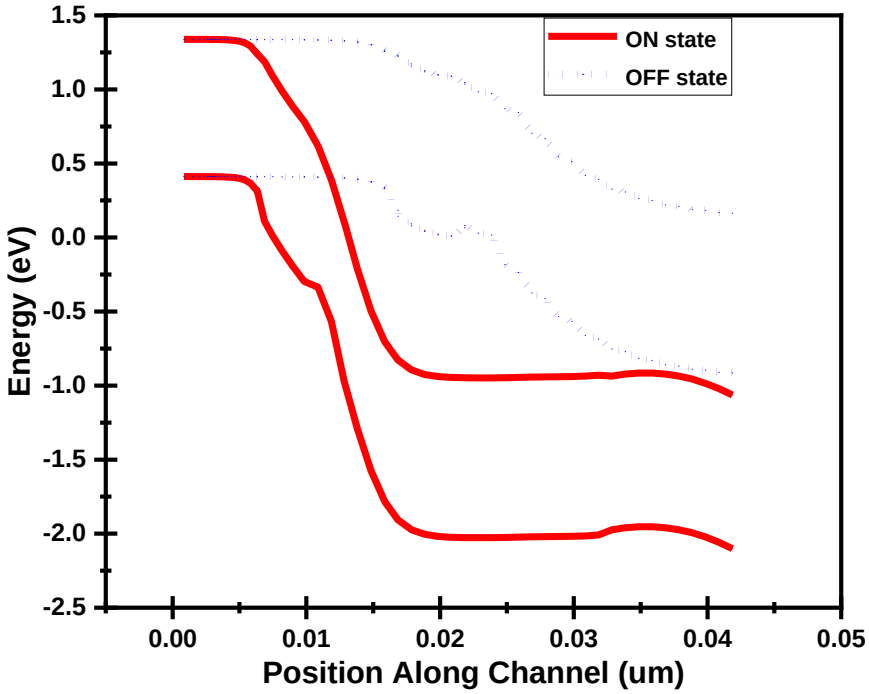

Fig. 9. Energy band diagram of PE-DMTG-TFET in ON (solid line) and OFF (dotted line) state

7 Result and Discussion

"By using the Wentzel-Kramers-Brillouin (WKB) approximation an expression for transmission probability (T_{WKB}) for TFET has been derived for the tunnel barrier as a triangular-shaped potential barrier [25]".

$$T_{WKB}=\exp\left(\frac{-4\sqrt{2m^*}}{3q\hbar F}\right)\times E_g^{3/2}(1)$$

Where q is the electronic charge, ħ is the reduced Planck's constant, F is the absolute electric field in the depletion region from the source to channel, E_g is bandgap of semiconductor and $m^*$is the"tunnelling effective mass". The basic motive is to enhance the absolute electric field near the source-channel junction (The Tunnelling junction), which increase the band to band tunnelling current.

This effect was previously accomplished by introducing dual-k spacers between the gate-source.We use a pocket at the source-channel junction that performs the same purpose of improving the electric field assisting tunnelling. There is a substantial decrease in the tunnel barrier of pocket dopedDMTG-TFET in ON-state as compared with DMTG-TFET.It, therefore, demonstrates that DMTG-TFETpocket engineering can prove to be a great alternative for improving the performance at lower node technologyFigure-10. For DMTG-TFETstructures with two different states (ON-OFF), the correlation of conduction and valence band energy is illustrated in Figure 11.The structure in ON state shows reverse band-bending at the channel drain barrier side that illustrates the impact of the same reduction in ambipolar current. It is also apparent that the valence and conduction bands are becoming parallel to each other along the drain side, negating the further chances of any ambipolar conduction. The potential distribution has been shown in Figure 13 at the increasing gate voltage. It can be noticed that with the introduction of P+ heavily doped pocket the amplitude of potential rises very sharply due to the reduction in barrier width. At the tunnel junction, there is a steep rise in potential, except it remains constant over a major part of the channel.

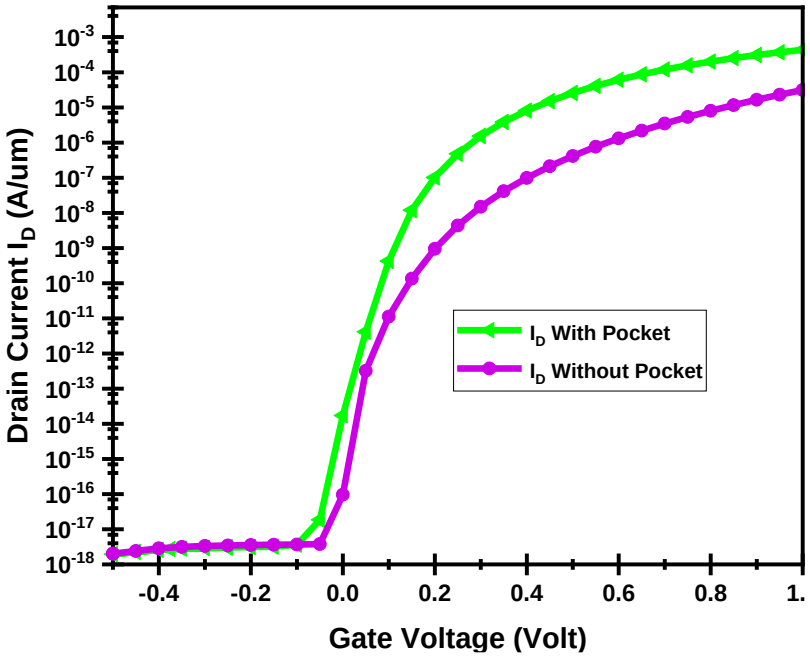

Fig. 102. ID Vs VGS characteristics of the pocket doped and without any pocket doped device

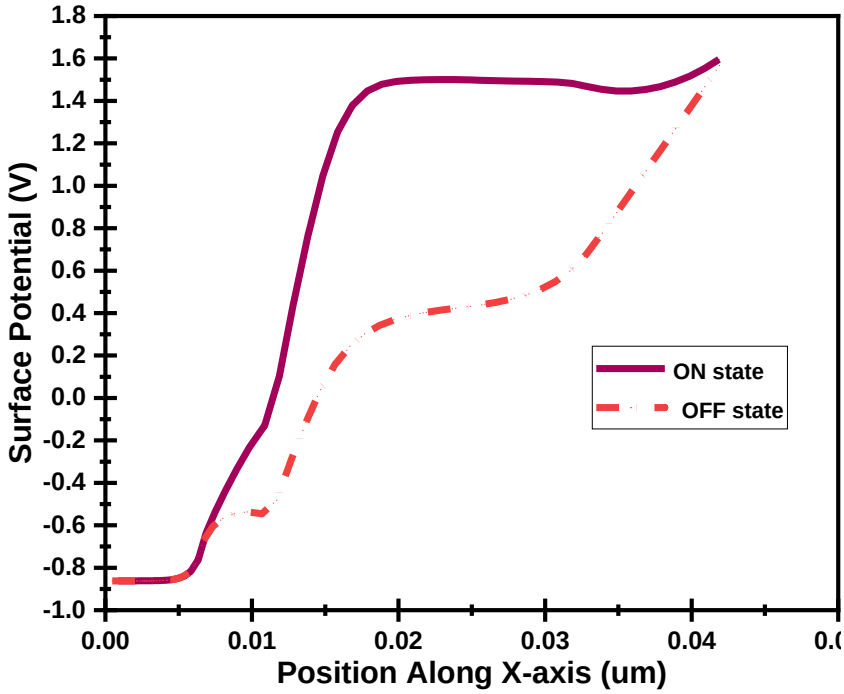

Fig.11. Results based on the simulation of surface potential distribution at ON (solid line) and OFF (dotted line) states

In Figure 12 I_D Vs characteristics of DMTG-TFET and pocket doped DMTG-TFET are compared and here the pocket doped TFET gives superior current as compared to DMTG-TFET at the same applied voltages with I_{OFF} $=3.307 \times 10^{-18}$(A/um), $I_{ON} = 4.67 \times 10^{-3}(A/um)$, $^{Ion}/_{Ioff} = 3.15 \times 10^{14}$ and SS=25.8605 (mV/Decade).

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8 Conclusion and Future Scope

In this paper, the structure of DMTG-TFET was taken and optimized for dimensions and doping concentration. After performing work-function engineering on the proposed device for a fixed gate and control gate, the device shows the excellent subthreshold slope, negligible ambipolar current and high I_{ON}/I_{OFF} ratio at short channel length. Finally, P+ pocket doping on the source side makes it more beneficial than the conventional proposed device. Compare to the conventional DMTG-TFET the proposed P+ pocket doped DMTG-TFET is shown to have higher I_{ON} (~12-15 times) and a good subthreshold swing (~ 25 mV/decade), that makes it an appealing device for forthcoming low power device application.

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