Novel Non-planar Structures of TFET Device to Enhance Performance

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Abstract

This paper reviews the development of various structures of Tunnel Field Effect Transistors. In order to enhance the on-state current and decrease the short-channel effects, various non-planar structures were designed. Among all these non-planar structures, DGDM-GeOI Vertical TFET structure not only provide the benefits of performance enhancement but also fulfill the requirement of reduced footprint of the device.

Keywords: Tunnel Field effect transistor (TFET), Vertical Tunnel Field Effect Transistor (VTFET), short channel effects(SCE), band to band tunneling (BTBT), Figure of Merit(FOM), average subthreshold swing(SS_{avg}), Subthreshold swing(SS).

1 Introduction

With the continual advancement in technology, the devices are constantly scale down to enhance the speed, efficiency and integration density. As the MOSFET continuously scale down, it reaches to its fundamental physical confinements due to presence of some short channel effects [1-2]. The biggest serious reason to limit the downsize of MOSFET is the increase in leakage current [2]. Different types of leakage current components: (a) Drain bias induced, (b) Direct tunneling between source and drain, (c) subthreshold, (d) gate oxide leakage current; these all are become vital for consideration for future devices. To overcome the drawback of SCE and source-drain off current of conventional MOSFET, number of novel non-planar TFET structures are reviewed in this paper.

2 TFET Structure and Operation

In the past few years, a low power device i.e., TFETs have been proposed which is based on a band to band tunneling (BTBT) injection mechanism with the intend of achieving a SS lesser than 60 mV/dec. limit at 300 K[3-5]. This device further helps to overcome the various bottlenecks that are present in MOSFET[6-10]. TFETs are basically a p-i-n diode, where the BTBT occurs parallel to the oxide-silicon edge. Fig. l(a) represents the schematic of a conventional lateral TFET. Fig. l(b) represents the band diagrams at the OFF and ON conditions. The tunneling barrier is so large when $V_g<V_t$ that there is no significant tunneling current is flowing through the device excluding a leakage current. The tunneling barrier width is so small when $V_g>V_t$, that it permits BTBT to take place. This tunneling current similar as ON current, in this tunneling take place collateral to gate oxide. However, the subthreshold swing is lower than 60mV/dec, but the estimated gate control of the device is weak. Gate control improves the performance of the device. With the intent to improve the gate control further new structures are exploited.

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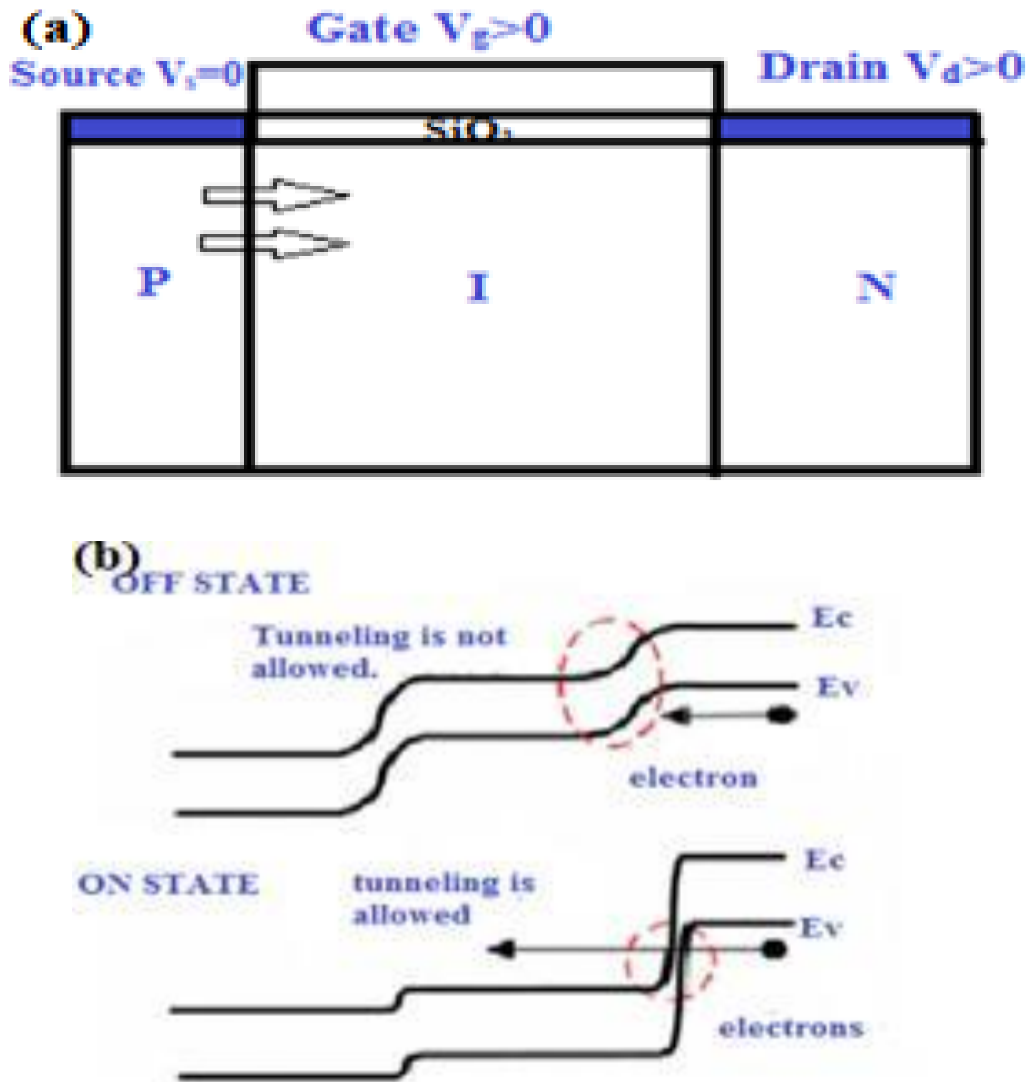

Fig.1: (a)represents the schematic of conventional TFET, (b) shows the Off and On condition band diagram of Lateral TFET respectively [3].

3 Novel Structures to Boost up I_{on} in Analog Low Power Devices

In order to improve the performance of analog devices different structures of TFETs are developed on the basis of shape of gates, regions and materials that are discussed below:

3.1 Raised Source TFET

In this paper, author proposed a raised Ge-source TFET [11-15]. High I_{on}/I_{off} ratio(>10^6) and steeper subthreshold slope is achieved by using fully elevated Germanium source device which is shown in fig.2. An improved energy delay performance obtained in this device in comparable with planar devices or partly raised TFET device. The transfer characteristics of Raised source Ge-TFET shown in fig.3.

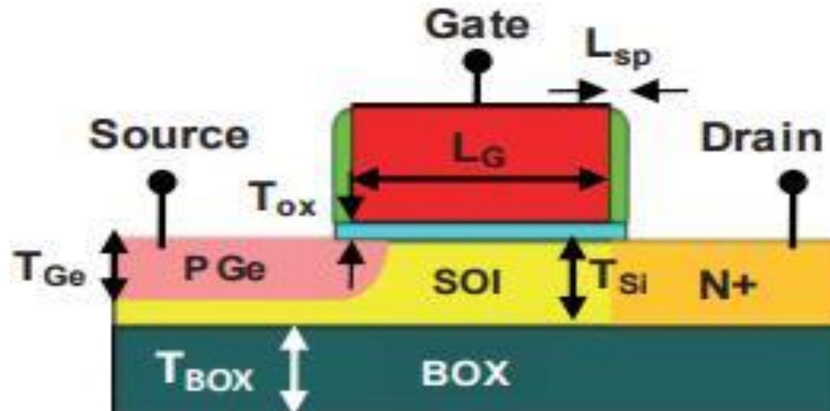

Fig.2: Cross-sectional view of a Raised source Ge-TFET[11]

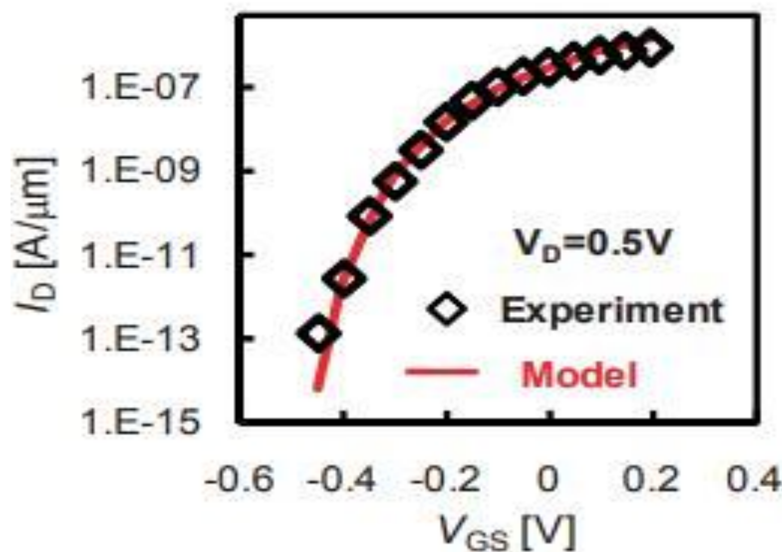

Fig.3: Transfer characteristics of Raised source Ge-TFET [11]

3.2 L-shape Gate TFET

In this paper, author proposed a L-shaped gate TFET (LG-TFET) [16] and examined through SILVACO TCAD tool which is shown in fig.4. Here tunneling junction is orthogonal to the channel path that enables the employment of a comparatively huge tunneling region. Due to U-shape channel, channel region primarily allocates in the upright direction, decreasing the device area. The n+ pocket is incorporated in the middle of the source and the intrinsic regions to enhance the device performance. By means of the L-shape gate, U-shape channel, and the incorporation of pocket, the total performance of this device is improved. The obtained I_{on}/I_{Off} for the device is ~10^{10}. The obtained transfer characteristics of LGTFET is shown in fig.5.

3.3 U-shape Channel TFET

A U-shape-channel TFET (UTFET) with a SiGe source area is simulated by TCAD simulation tool [17]. The expanded tunneling area and improved tunneling rate intensively enhance the on current when the device is in on condition. In the meantime, the off current of UTFET is reduced due to increased channel length. To further improve the on current of UTFET, delta layer is introduced underneath the source region. The incorporated delta layer appreciably narrows the BTBT path, increases tunneling area, hence improves the tunneling current of this device.

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The SS_{avg} of this device is 58 mV/dec. By means of the SiGe-source UTFET with a delta layer, some advantages are realized like: small off current, large on current, and ultra-low Subthreshold swing. To realize the performance of this device, energy band diagrams of this device are considered in fig. 7. The obtained I_{ON}/I_{OFF} ratio for this device is ~10^8.

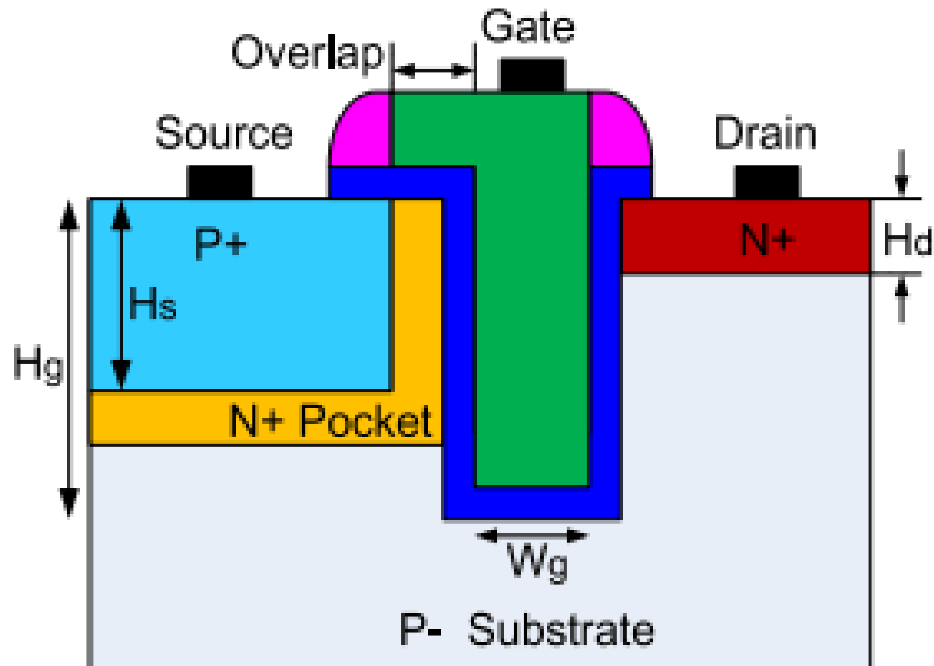

Fig.4: Schematic of the LG-TFET[16].

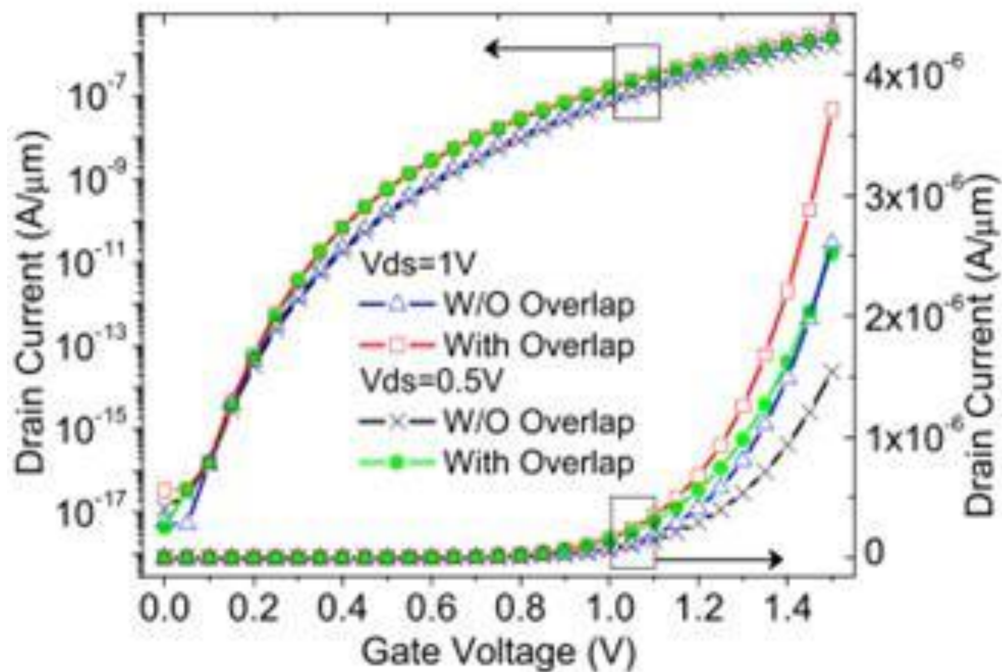

Fig.5: Transfer characteristics of the LG-TFET[16].

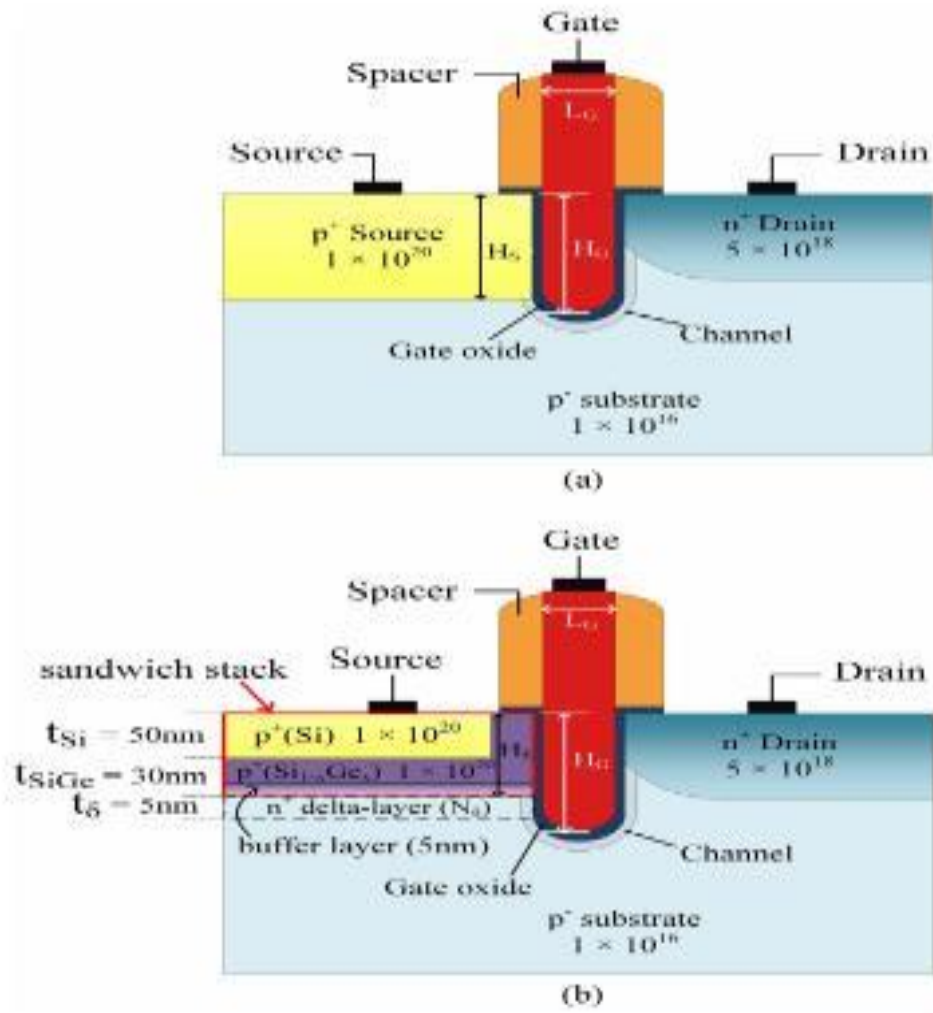

Fig.6: Schematic of U-shape TFET[17].

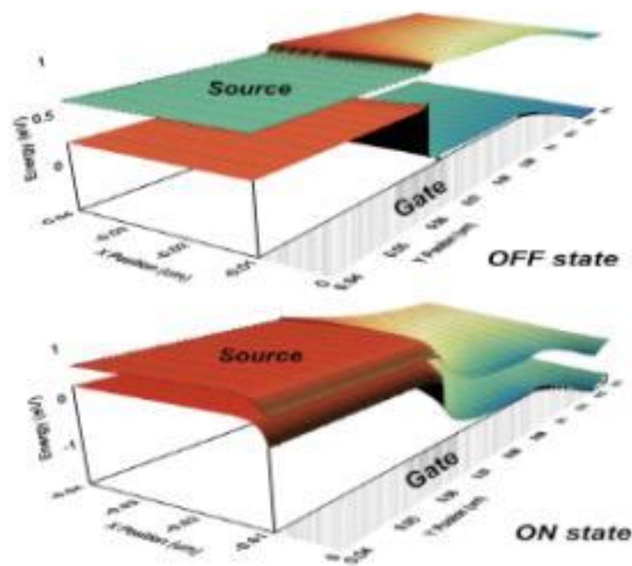

Fig.7: Band diagrams of SiGe-UTFET structure[17].

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3.4 Symmetric U-shaped Gate TFET

In this article, Shupeng chen proposed a heterojunction symmetric U-gate TFET(SUTFET) device. This device has a small off-current of 3.1 pA/µm and a high on-current of 13.5 µA/µm with a min. SS of 152 mV/dec. and I_{on}/I_{off} of $4.4x10^6$ is obtained. In contrast to UTFET, this device has long channel length. It helps in restraining short channel effects. The schematic of SUTFET is shown in fig.8 [18]. The obtained results of this device are: I_{ON}/I_{OFF} is 4.4×10^6 and minimum SS is 15.2 mV/dec.

3.5 T-shape Gate TFET

In this paper, the T- shape gate dual-source TFET (TGTFET) device is proposed and simulated on TCAD software. The tunneling junction area become double in case of TGTFET as compare to UGTFET and LGTFET. In T–shape gate, gate overlap increases the BTBT rate. The characteristics shown in fig.9 shows that gate overlap increases the ON-current[19]. The obtained I_{ON}/I_{OFF} for this device is 6.7×10^{10}.

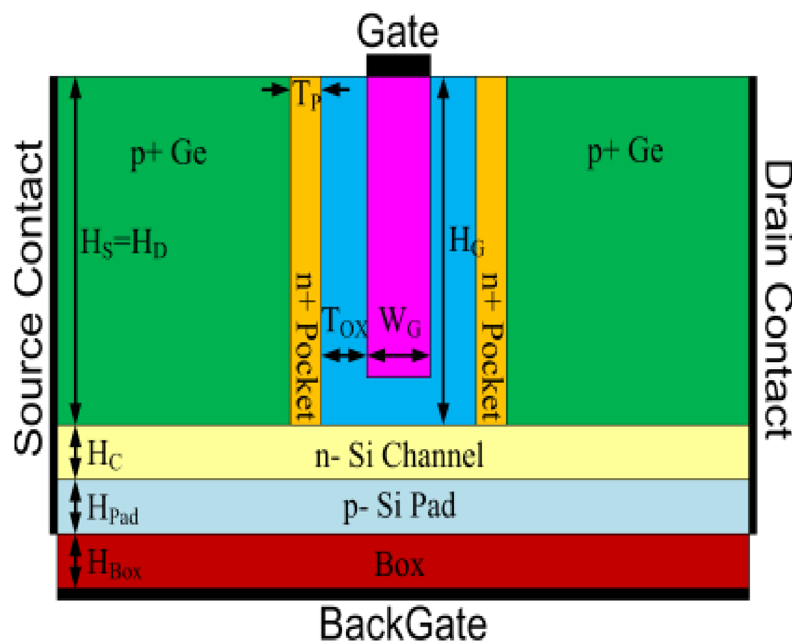

Fig.8: Schematic of symmetric U-shape TFET[18].

3.6 T-shape TFET

In this paper, author reported an InP/In0.53Ga0.47As heterojunction-based T-shape TFET(TTFET)[20-21] device that provides high On-current due to increased tunneling cross-sectional area. Ambipolarity was also reduced in this device due to gate-drain overlap architecture. The cross-sectional view of TTFET is shown in fig.12. The superior electrical characteristics was found in TTFET with respect to L-shaped TFET (LTFET) that is represented in fig.13. The obtained I_{on}/I_{off} for this device is $5.1x10^8$.

3.7 Two source TFET

In this paper, author proposed a SOI-based TFET with two source regions (TSRs) [22] which is shown in fig.14. The integration of the TSR increased the actual tunneling area which further increased the on-current of this device. Isolator oxide which confined the leakage current [23-26] at a smaller value as this prevents the direct tunneling. The distinctive FOM of this device is its current ratio, i.e., $\sim 9 \times 10^{10}$. The influence of channel doping on TSR TFET is shown through transfer characteristics that is represented in fig.15.

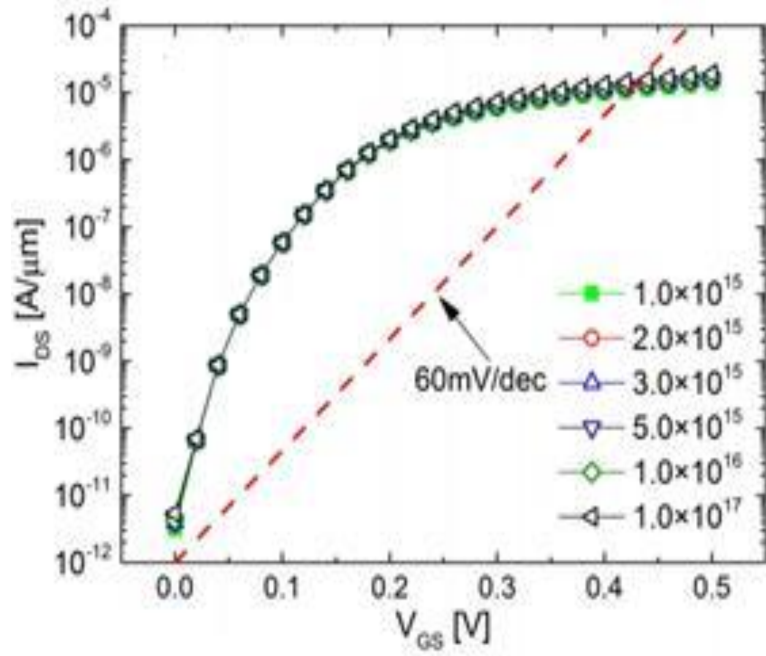

Fig.9: Transfer characteristic with different channel dopings[18].

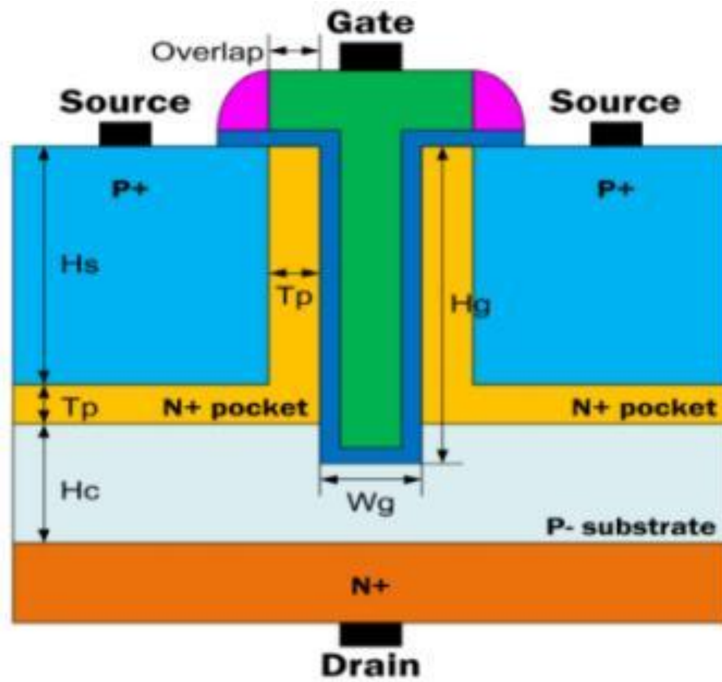

Fig.10: Schematic of T-shape gate TFET [19].

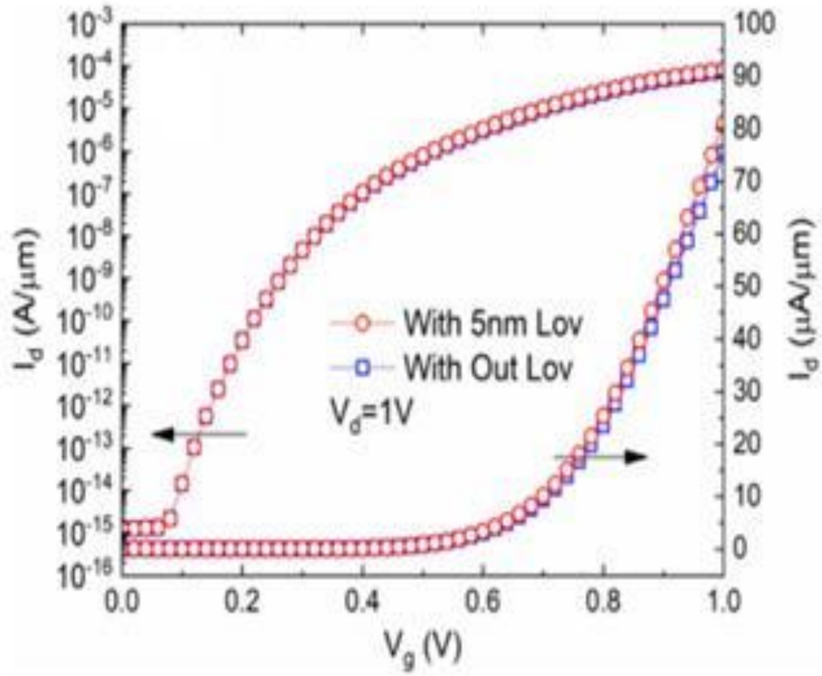

Fig.11: Variation of drain current w.r.t. gate voltage [19].

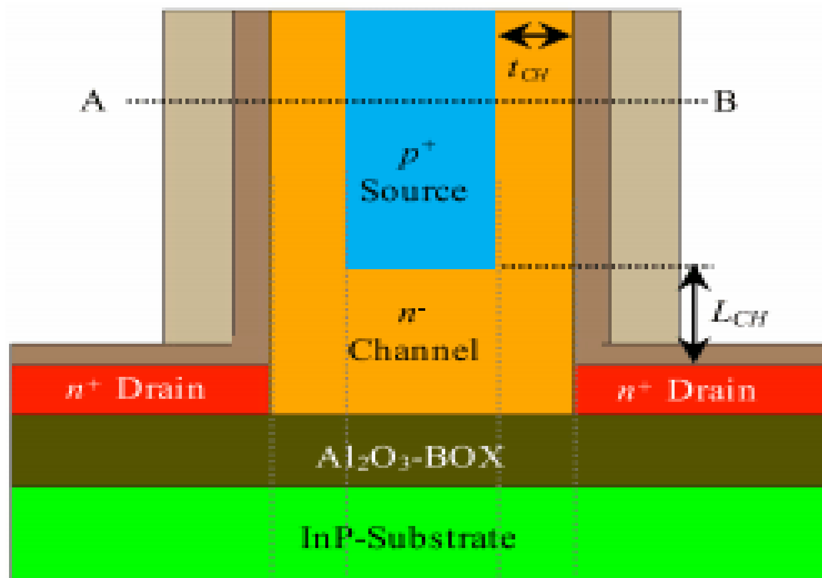

Fig.12: Cross-sectional view of TTFET[20].

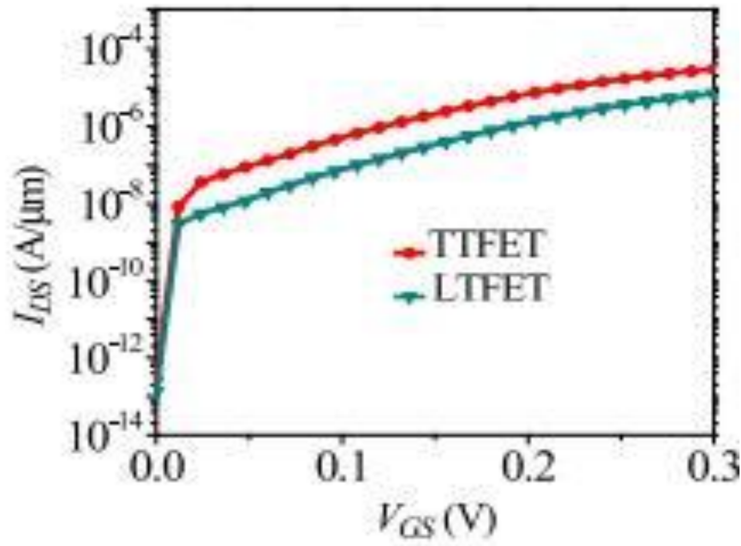

Fig.13: Comparison b/w TTFET and LTFET through Transfer characteristics[20].

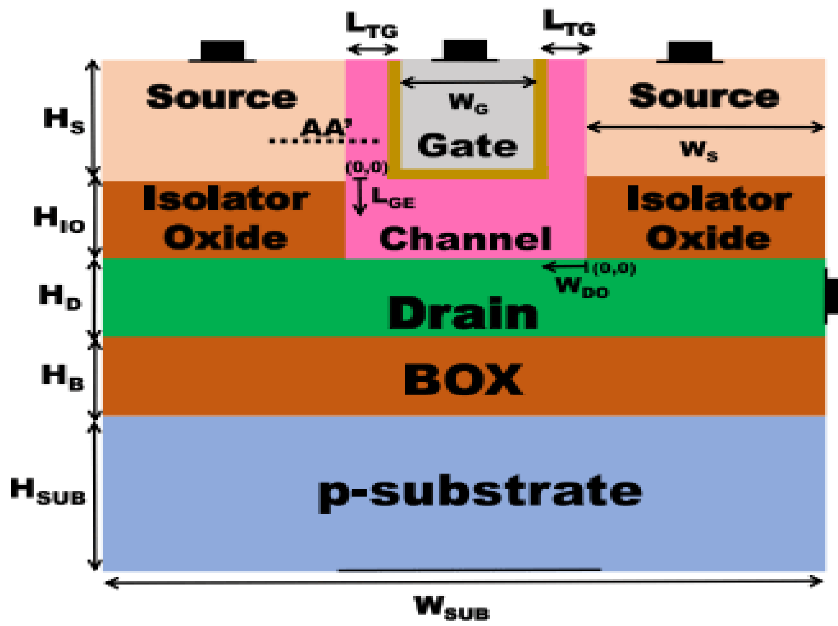

Fig.14: Schematic of the proposed SOI-TSR TFET[22].

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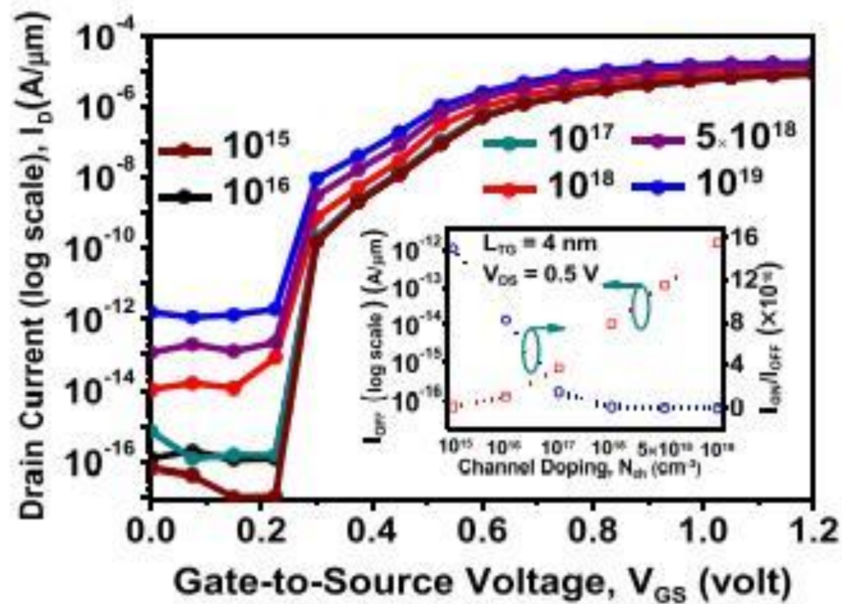

Fig.15: Influence of channel doping on the TSR TFET device [22]

3.8 Vertical TFET

In this letter, author proposed a double gate dual material germanium on insulator Vertical TFET (DGDM-GeOI VTFET) device [27]. The VTFET [27-28] has several merits in comparison to LTFET i.e., steeper subthreshold slope. Here gate metal work-function engineering, material engineering and tunneling mechanisms enhances the performance parameters of the device. The obtained I_{on}/I_{off} and SS_{avg} of this device is $3.51\text{x}10^{11}$ and 14.684 mV/dec. Further, this vertical device has small footprint as compared to lateral devices. The schematic and transfer characteristics are shown in fig.16 and fig.17 respectively.

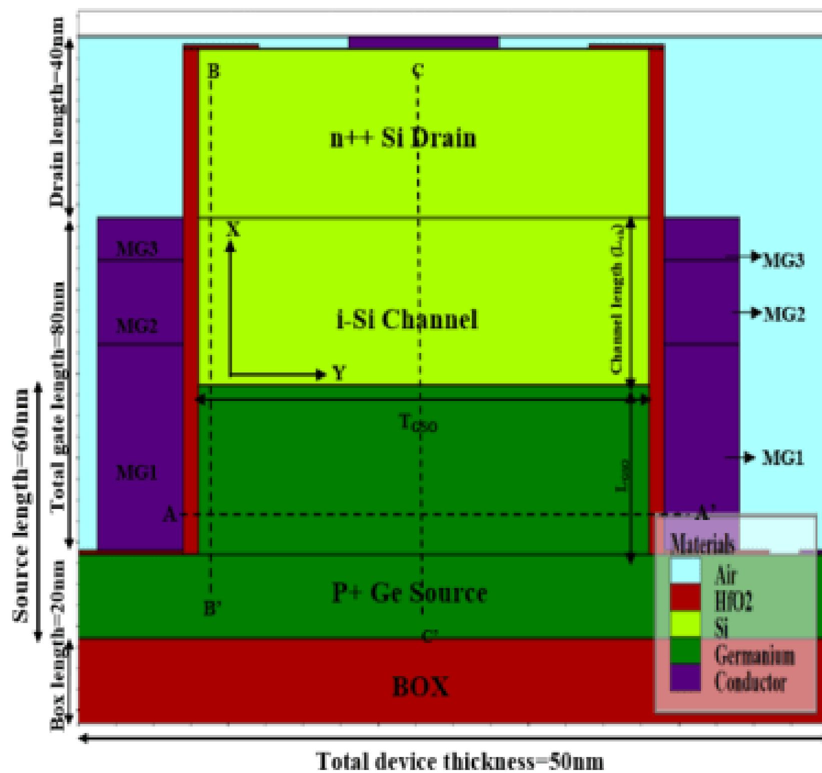

Fig.16: Schematic of DGDM-GeOI VTFET [27].

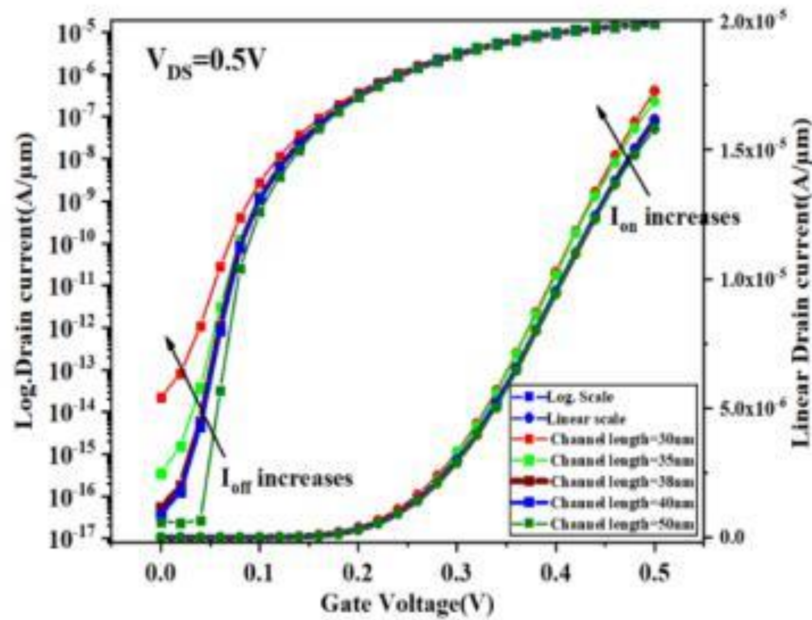

Fig.17: Variation in transfer characteristics of DGDM-GeOI VTFET at different channel lengths[27].

4 Conclusion

A comprehensive review of TFET is prepared in this paper to give a clear idea about the current status of the development of TFET. This study shows the impact of shape engineering, material engineering and tunneling mechanism on the subthreshold swing, I_{on} current, I_{on}/I_{off} ratio and leakage current. Further these different types of structures suppress the various short channel effects which are earlier present in MOS. Among all these structures, DGDM-GeOI Vertical TFET structure not only provide the benefit of highest I_{on}/I_{Off} ratio at V_{gs}=0.5V but also fulfill the requirement of reduced footprint for a device.

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