Fabrication Process of MBCFET and its Characteristics

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Abstract

This paper demonstrates the fabrication process of a novel 3-D multibridge-channel MOSFET, using the conventional CMOS process. It contains a comparative study of I-V characteristics between planer MOSFET and MBCFET. It shows how conventional MBCFET has a disadvantage of poor gate bias control and leakage characteristics and how it can be avoided by using core insulator.

Keywords: Multibridge-channel MOSFET (MBCFET), Chemical mechanical processing (CMP), Cross stacking.

1 Introduction

Moore's law predicted in 1965 that transistors per chip doubles every year, which than altered to doubling the number of transistor per chip in about 18 to 24 months. As the number of transistors per chip increases the transistor size decreases, and with decrement in size of transistor there comes a huge difference in their efficiency, speed and power requirements. It is a challenge to maintain the desired efficiency and response with each technological increment. According to International Technology Roadmap for Semiconductor (ITRS) 2002 the transistor gate length decreases almost 15% every year but current drivability requirement remains the same for the lesser operating voltages.

So to overcome these challenges with reduction in gate length of the transistor, many alternates have been introduced one of which is Multibridge-Channel MOSFET (MBCFET). But there is fabrication limit also and one solution to fabrication limitation is novel process technology, in this process the main focus is to avoid the limitations related with the lithography process, other available options are using different type of gate electrodes and dielectrics, by which the gate poly depletion is reduced as well as the gate leakage current. [1]

2 Transistor Fabrication Technology

The fabrication process flow for a MBCFET is shown in Fig. 1. A very significant effect which affects the transistor operation and its performance is parasitic transistor operation in semiconductor well, and to get rid of this effect, channel isolation ion implantation is applied before the epitaxial growth of multiple Si0.8Ge0.2 and Si layer. The width of these layers must be lesser than a critical thickness to avoid any kind of lattice imperfections. By controlling the number of these alternate layers the number of channels can be controlled which in turn results in control over the current drivability of the MOSFET. [1] [2]

For etching of epitaxial layers to make source and drain region a SiO2 layer is used as a hard mask. After this etching, a narrow S/D extension layer is formed which is then doped by tilted ion implantation.

Filling for source and drain region is done by depositing poly-Si layer. A thick SiN layer is deposited and flattened using CMP. After the deposition of SiN layer the dummy gate layer of SiO2 is removed. [2]

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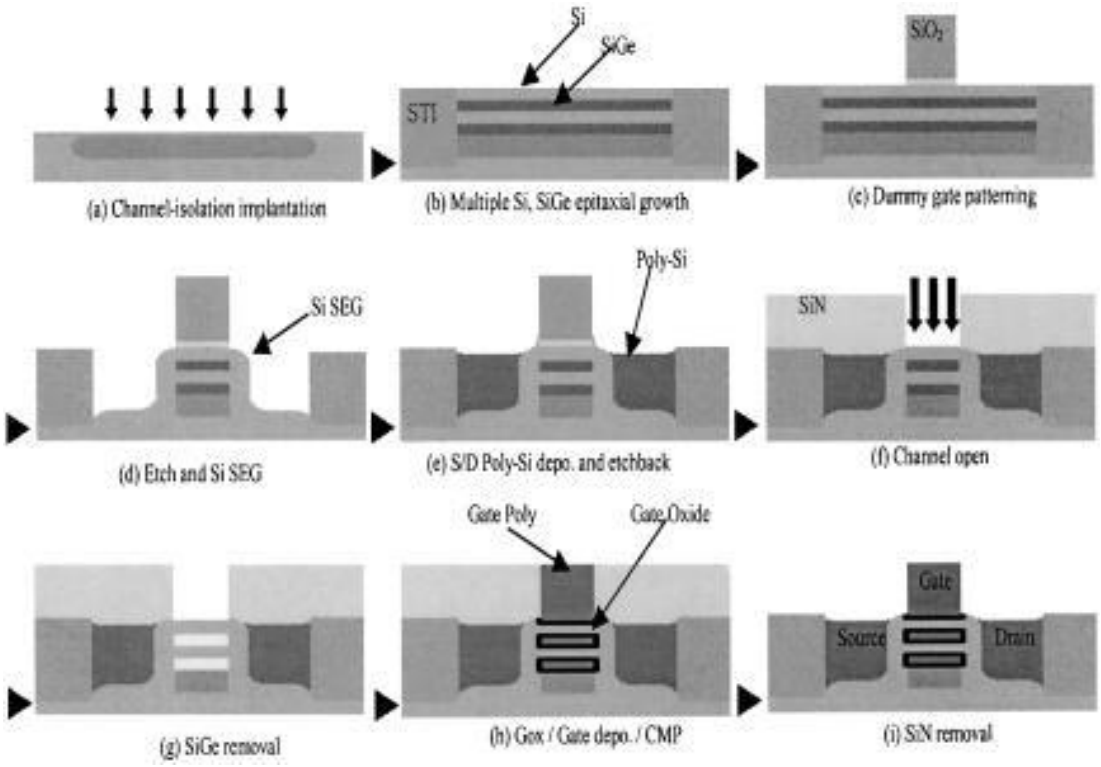

Fig.1: MBCFET Fabrication Process [1]

To adjust the threshold voltage (Vth), the multibridge-channel region underneath this removed dummy gate layer is implanted with multiple energy. Now, by using SiN and Si hard masks, the Si0.8Ge0.2 layer is etched anisotropically. This process is made highly selective towards Si0.8Ge0.2 over Si. The selectivity ratio taken here is higher than 300:1. To form the gate for n-channel MBCFET, gate oxidation is done using N2O, highly N-type doped poly-Si deposition, planarization using CMP and SiN deposition is done. [1]

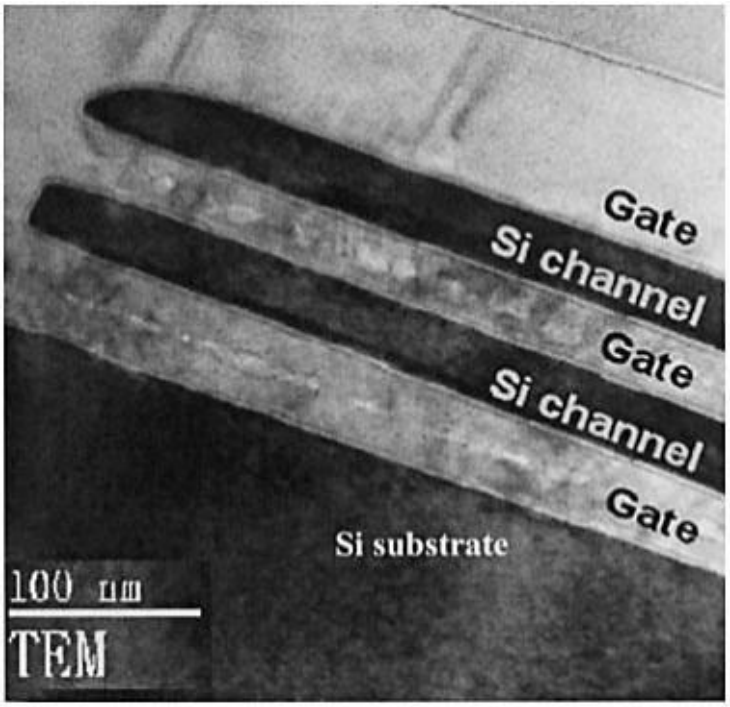

Fig.2: Final profile of MBCFET [1]

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3 Transistor Characteristics

Fig. 3 and Fig.4 shows the Drain current (ID)-Drain voltage (VD¬) and the Drain current (ID)-Gate voltage (VG) characteristics of the n-channel MBCFET with width to length ratio k=0.2. If a comparison is done between the threshold voltages of MBCFET (which is 0.1 V), and of planar FET voltage (which is 0.45 V), then it is clear that MBCFET has a lesser threshold voltage (Vth) than planar FET.

This difference occurs due to the thin body effect which is completely wrapped around by the gate. For an n-channel MBCFET with channel length of 240 nm and width of 5 μm, the subthreshold swing can get as low as 60 mV/dec [3], which is very near to the ideal performance. This near ideal performance is also a result of the thin body, wrap around by the gate. The current drivability of MBCFET (which is 38 μA/μm for VGS=VDS=1 V) is higher than planar FET (which is 2.9 μA/μm for VGS=VDS=1 V). [1] From the graph shown in Fig.3 it is clear, that the planer MOSFET has a significantly lesser amount of current drivability.

This significant difference happens because of the vertically stacked multi-bridge channels (MBC) of MBCFET. [1]

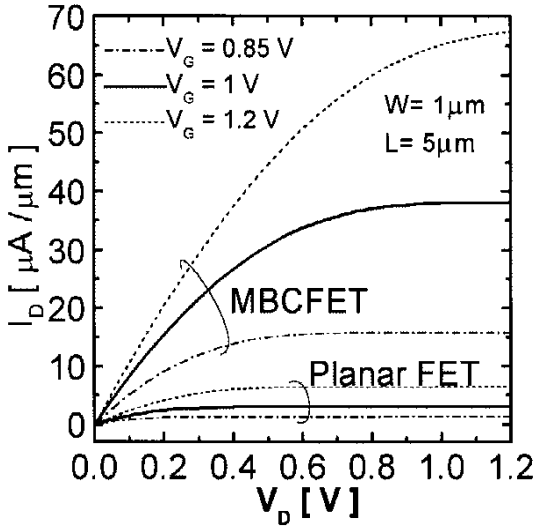

Fig.3: Drain current (ID)-Drain voltage (VD) characteristics of MBCFET [1]

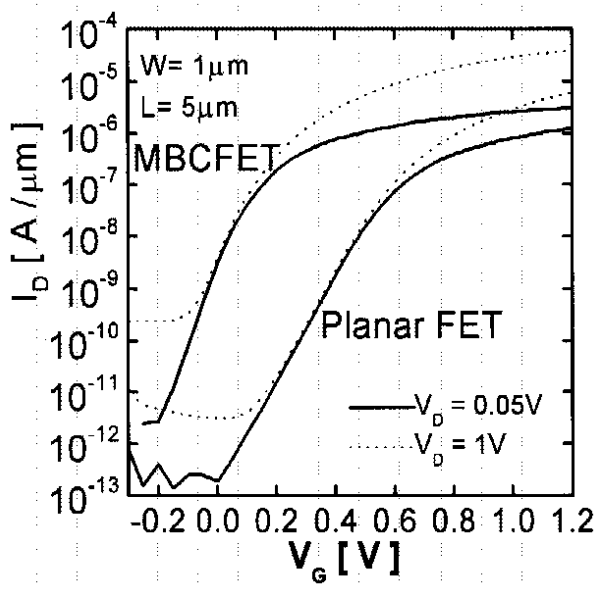

Fig.4: Drain current (ID)-Gate voltage (VG) characteristics of MBCFET [1]

4 Leakage Profile Improvement

By adding a core insulator layer, the leakage profile of the conventional MBCFET can be improved. Fig. 5(a) and 5(b) depicts the variation in electron current density, the cross section view of electron current density for conventional and core insulator MBCFET is shown respectively. The core insulator MBCFET has a narrow insulator (oxide) layer in the middle of the channel and the channel including the core insulator layer is surrounded by HfO2 gate oxide and metal gate. [4]

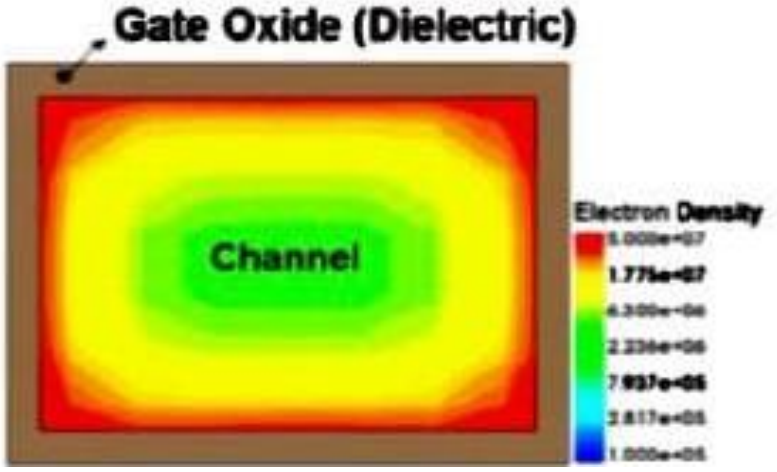

Fig.5: (a) Conventional MBCFET electron current density [4]

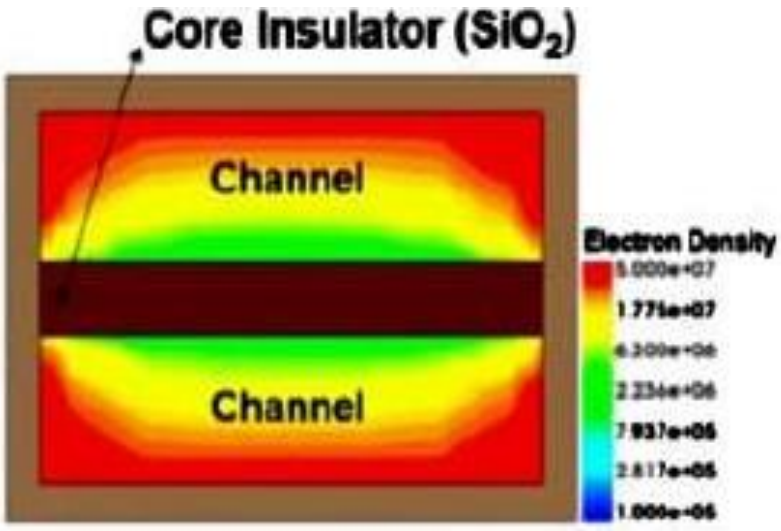

Fig.5: (b) Core insulator MBCFET electron current density [4]

Because of the cross stacking of Si and Si0.8Ge0.2 layers and an insulator layer between Si and Si, the distance between gate electrode and channel increases due to which the effect of gate biasing on the channel reduces and further results in poor gate controllability and leakage characteristics, which clearly can be depicted from Fig. 5(a), i.e. as the distance from gate increases the electron density reduces. This problem is solved by removing this poor gate control area using core insulator as shown in Fig. 5(b). Adding the core insulator in the MBCFET results in improved electrostatic properties. [1] [4]

5 Conclusion

The paper shows the fabrication process of the multibridge-channel MOSFET (MBCFET), and how adding multi-layered channel results in increment of current drivability of the MBCFET device. Comparison of

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current-voltage characteristics of MBCFET with planer MOSFET shows how significant this change is. Although, because of this cross stacking, the gate control over channel degrades, but this problem is overcome by adding a core insulator. There are still areas of improvements are present in MBCFET which are expected to be entertained in the future as the demand for performance increases.

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