A Literature Survey on Tunnel Field Effect Transistors

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doi: https://doi.org/10.21467/proceedings.114.65

Abstract

TFET or Tunnel Field Effect Transistor in recent times has been the center of attraction of vast number of researcher's despite of having minute subthreshold slope and excessive Ion/Ioff ratio. It is known that TFETs are much more immune to short-channel effects and fluctuations of random dopants in comparison to their MOSFET counterparts. TFETs are actually gated p-i-n diodes having tunneling current flowing between source and channel bands. In this paper deep rooted literature review has been done scanning each and every aspects of TFET including the variations of performance with different parameters. The paper finally gives a picture on the recent progress of TFET in different aspects such as from subthreshold swing to a significantly lower leakage current and high on current .For the simulation curves Nanohub.org was used as a tool . Lastly different types of TFET in respect of doping to symmetry and also gates are compared.

Keywords: Tunnel Field Effect Transistor, Tunneling, Subthreshold Swing, Ultra Thin Body Double Gate TFET

1 Introduction

Complementary Metal Oxide Semiconductor (CMOS) is the most well-liked switch as it exhibits certain properties like the enhancement in drive current and the cut ff frequency with the scaling down [1] of the semiconductor devices, thus making suitable to be used extensively for switching purpose .Scaling of CMOS [1] based semiconductor devices is mainly governed by Moore's law [2,3] which states that " the number of devices on a single chip will double in every eighteen months " In recent times due to scaling down the dimension of Complementary Metal Oxide Semiconductor (CMOS) has been brought down to the nanometre range thus making the power management and lithographic process very cumbersome . Major drawback of the conventional MOSFET is that the subthreshold slope obtained remains fixed when we plot I_{DS} -V_{GS} on a log-in scale to eradicate the above-mentioned problems of the conventional MOSFET a new device known as the Tunnel Field Effect Transistor [4,5] i.e., TFET came into existence. Some of the salient features of TFET are as follows

i) Band-to-band tunneling [6] mechanism is used which helps in reducing the leakage current.
ii) The value of Sub threshold slope is lower than 60mV/decade [7,18] .
iii) It is mainly used in applications which requires low power.
iv) It has a high ON/OFF current ratio.
v) Helps in reducing the Short Channel Effects [8].

Basically, we want a device which is analogous to the FET i.e., Field Effect Transistor. In the new device the tunnel current must flow when we alter the gate voltage the Band-to-band tunneling mechanism [6] should be used during the activated state and during the alteration of ON/OFF state. The main target of this particular device is to realize the low amount of OFF state current and the minute value of the sub threshold swing should be beyond 60mV/decade which is fixed for the conventional MOSFET and it is not flexible , therefore it is not possible to manufacture any transistor with an ON – state having a small V_g .

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Proceedings DOI: 10.21467/proceedings.114; Series: AIJR Proceedings; ISSN: 2582-3922; ISBN: 978-81-947843-8-8

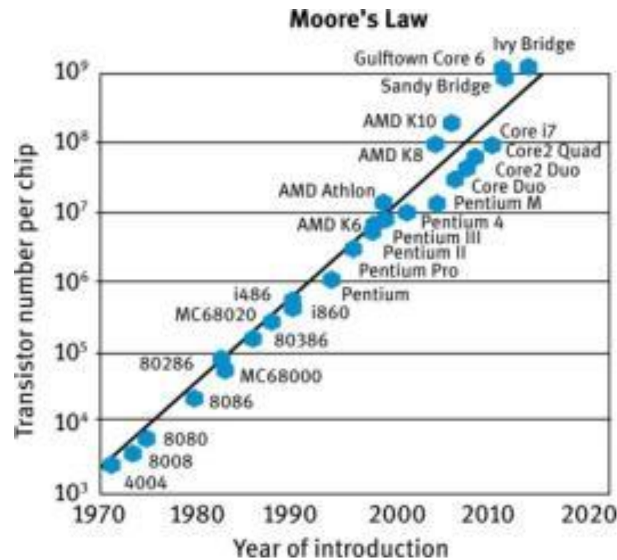


Fig 1 : Moore's Law graph of no. of components on a chip vs year -No. of components on a chip doubles after every two years. This graph shows the most recent scenario till the year 2020 [2]

The Tunnel Filed Effect Transistors [5,6] as the name suggests is basically based on the principle of Band To Band Tunneling [6] . As it is based on the micro particles the quantum tunneling comes into the picture. It's an asymmetric device as the doping is different for the source and the drain. This is the major difference to its MOSFET counterparts . In a TFET the device is PIN [9,10] type with the gate terminal in control of the intrinsic region's electrostatic potential. With the application of the gate bias there is an accumulation of electrons in the intrinsic region and as the gate bias is applied at a sufficient level there is an occurrence of Band to Band Tunneling [6] . An alignment of the conduction band occurs with valence band and there is a tunneling of electrons from the valence band of the P – region to the conduction band and there is a flow of current. Then when there is a lowering of gate bias the bands get misaligned and no current flows .

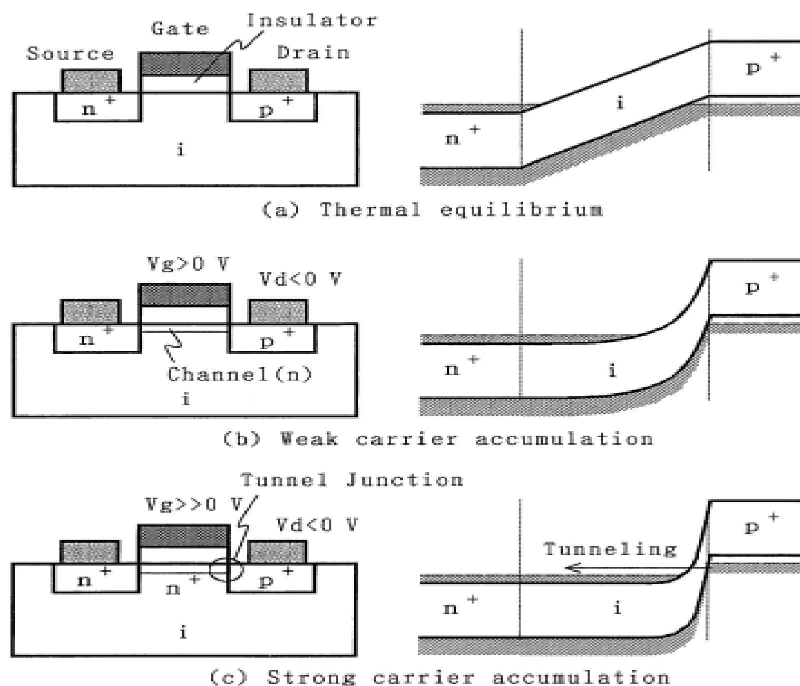


Fig 2 : Surface Thermal Transistor in three modes (a) Thermal Equlibrium , (b) Weak Carrier Accumulation , (c) Strong Carrier Accumulation. [11].

If we dig deeper into the basic of the Subthreshold Slope equation we can see that lower the technology nodes , steeper is the I_D Vs V_{GS} curve and lesser would be the off current which is shown in Fig 3 , where we have the I_d vs V_{gs} curve simulated from MugFET tool in NanoHub.org [12,13]. Also we can see that subthreshold slope [7,19] can be brought down to about 60mV/decade .

$$Subthreshold\ Slope = 60(1 + C_d / C_{ox}) \qquad (1)$$

To lower this we need to either get high value for C_{ox} or lower value for C_d .

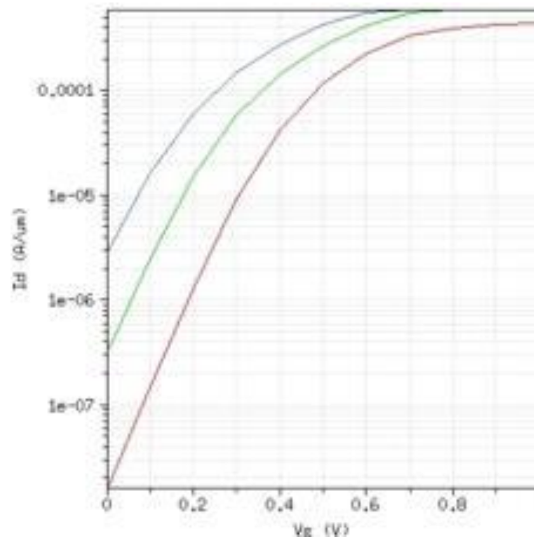
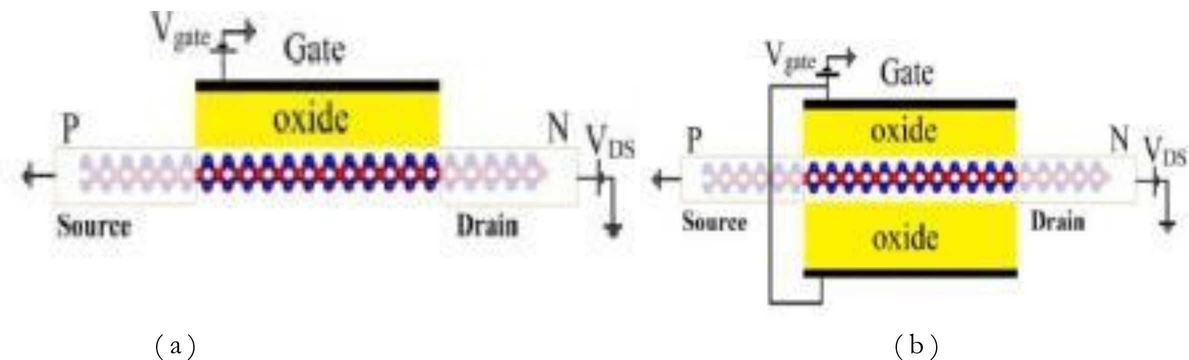


Fig 3: I_d vs V_{gs} curve for lower technology nodes showing lower value for I_{off} and very low subthreshold slope [13]

The Tunnel diode came into the scenario and from there was the introduction of the Surface Tunnel Transistor [11],the schematic figure of the same has been shown in Fig 2.The STT has got gate over its intrinsic region and resembles to that of a p-i-n diode [7] . The problem of the I_{off} larger value has been encounter with the SOI Technology , where the oxide thickness is increased to increase the depletion width and lower the depletion capacitance and then finally lower the subthreshold slope . TFET has got a few hiccups in the form of very low value of I_{on} to fluctuations in doping and also adding to that a big issue regarding ambipolar current [14,15] . In this survey paper we have review them and tried to bring the loopholes of TFET [16] and their solutions under one roof .

2 TFET Catagories, Loopholes and Solutions

TFETs can be divided into two types – the Conventional and the Junctionless Tunnel Field Effect Transistors .Next we move further to the issues encountered by them .



(a) (b)

Fig 4: (a) Ultra Thin Body Single Gate TFET, (b) Ultra Thin Body double Gate TFET.[17]

Proceedings DOI: 10.21467/proceedings.114
Series: AIJR Proceedings
ISBN: 978-81-947843-8-8
ISSN: 2582-3922

Taking into account different issues of TFET [16] we have got an issue of lower on current , solving this issue will lead to creating a huge amount of high electric field in source and drain region . If we need to mend the loophole it can be done by few steps of lowering the oxide thickness to thickness of silicon body . Adding to that doping of the source can also be increased .

Figure 4(a) and 4(b) shows the cross sectional view of Ultra Thin Body Single and Double Gate TFET respectively. These devices are considered and simulated in *NanoHub.org* [17] with device parameters taken as in Table I .

Table I .

L_{ch}	t_{ch}	K	V_{DD}
15nm	0.65nm	25	0.5V

L_{ch} = Channel Length ,t_{ch} = Channel Thickness , K = Dielectric Constant , V_{DD} = Supply Voltage

Then the t_{ox} have been varied from 3 nm , 10 nm , 15 nm and 20nm and it has been seen that the subthreshold slope of this particular device is approximately 42mV/decade, the channel length is 15nm and the oxide thickness is 3nm.

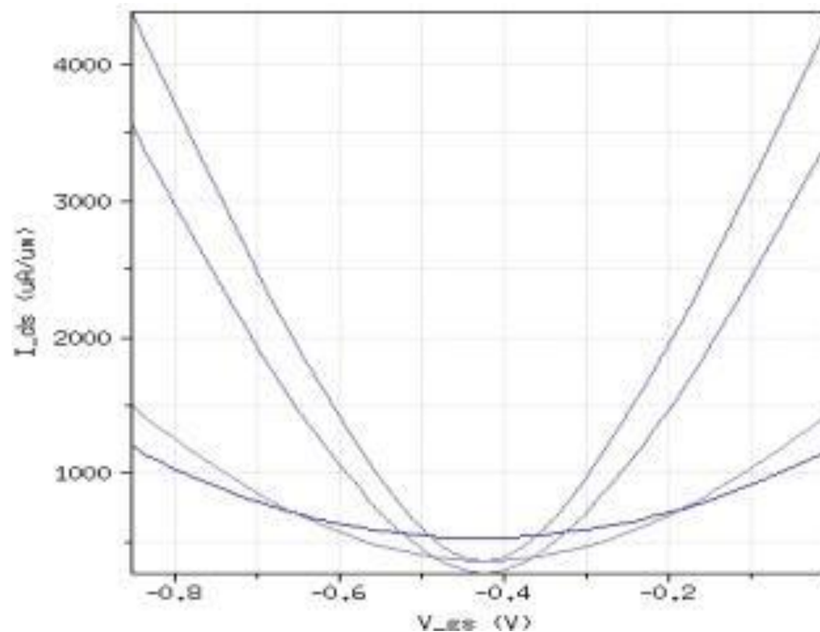


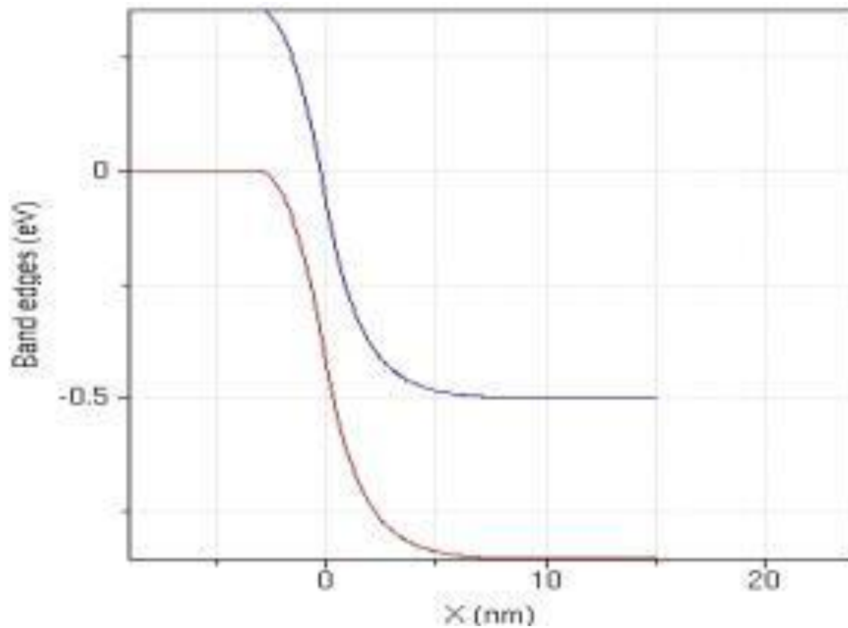
Fig 5: I_d vs V_{gs} curve for Tunnel FET Compact Model .[17]

It is noticed that as soon as the scaling of dimensions are done avoiding the V_{DD} scaling there is an enhancement in leakage power , then as soon as V_{TH} is reduced in order to push the gate overdrive voltage by I_{DS}-V_{GS} shift I_{off} is encouraged to grow .TFET has lower subthreshold swings [18] having a high value of I_{ON} / I_{OFF} .TFET is a kind of device which provides avenues to issues arose by huge scaling. For better performance we can lower the thickness of gate oxide and SOI layer, reduction in material of band gap channel and also have a better improvement in fabrication process .

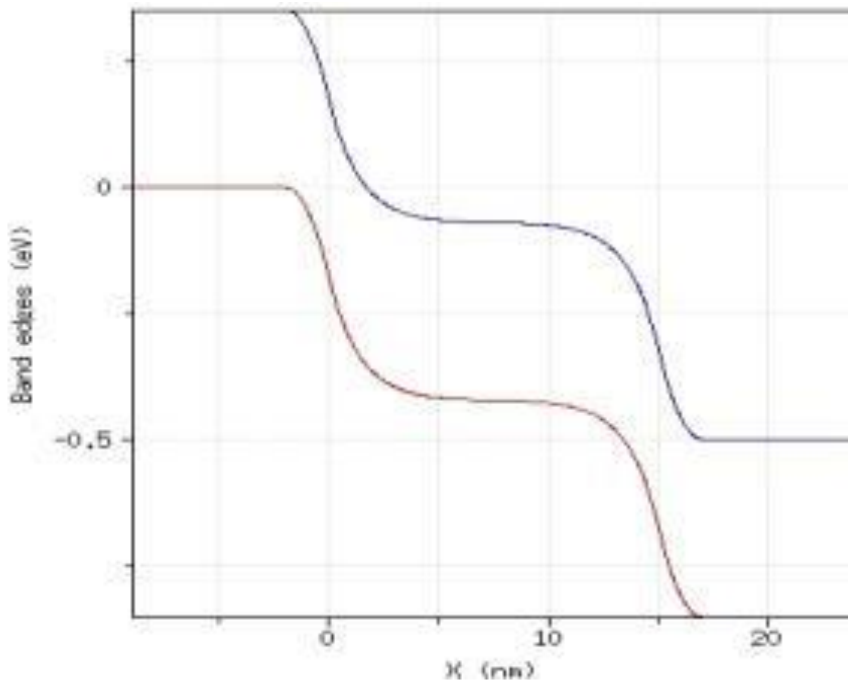
Next we turn on to the ambipolar current problem [14,15] whose remedy will lead to lowering of the electric field of channel and drain , then hinders the increasing of I_{on} therefore having the same issue of subthreshold slope [20] . In order to get through this issue research was done by trying to make a Tunnel Field Effect Transistor devoid of any overlap of gate and drain.This work at some point had a backdrop of lowering the chip density. This is where the Hetro Gate Dielectric Field Effect Transistor [21] has come into picture .

This model has the capability of compensating the ambipolar current without reducing the chip density also increasing the I_{on} . The high – K dielectric have been added to the source side enhancing the switching capability. The leakage current also gets reduced to a significant value.

In Fig 6 (a) and Fig 6 (b) the On and the Off state current of $E_c – E_v$ has been shown below simulated in *Nanohub.org* [6,8] for the devices considered in 4(a) & 4(b).The maximum value of the electric field will be seen along the x – axis in the energy band diagrams . The tunneling of the electrons takes place from source to drain with the push from higher electric field. In the I_{off} state the V_{gs} is very much lesser than V_{th} whereas in the I_{on} , its just the opposite.



(a)



(b)

Fig 6: (a) Ec-Ev ON State, (b) Ec-Ev OFF State [17]

Proceedings DOI: 10.21467/proceedings.114

ISBN: 978-81-947843-8-8
ISSN: 2582-3922

Finally we throw some light on the void of Random Doping Fluctuation . Now for proper uniform doping we need to get through few devices such as Junctionless , Polarity Based and Charge Plasma Based Field Effect Transistor [22].

JL-TFET [23] is denied of any metallurgical junction. It's heavily doped n-type with Si-Channel. This has no pn-junction either as in the lateral direction of the conduction layer there is no concentration gradient. So, it is easy to fabricate having better electrical properties and much lesser variable than that of MOSFET. .As there are no sharp doping gradients. The scalability is much better and more resistant to short channel effects. Still, there are some issues with I_{on} so we can use dual material gate for the same to improve it .Now in the Charge Plasma based TFET there is no need for doping . p^+ and n^+ regions gets induced in the Si body (intrinsic) by source and drain metal electrode with proper work functions . Source will get induced with holes if work function is high and drain to get induced with electrons if work function is low . In the absence of high doping concentration there is very less complexity in the fabrication process of Charge Plasma Based Tunnel Field Effect Transistor .

3 Conclusion

TFETs have outsmarted their MOSFET counterparts in respect to a much lower value of subthreshold swing to better immunity to different short-channel effects. Some backdrops have also been taken into account like: ambipolarity behavior , cost issues and low value of on-current . The values obtained is very less in comparison to the value 60mV/decade which is the standard value of the subthreshold slope of a normal MOSFET but the above parameters give us an option of using this device for switching purpose in our near future [24]. Inspite the overall performance of this particular device Also TFET has found place in applications of proper switching devices as well as memory devices [25].

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Proceedings DOI: 10.21467/proceedings.114

Series: AIJR Proceedings

ISBN: 978-81-947843-8-8

ISSN: 2582-3922