Comparative Analysis of Multiplications Technique Conventional, Booth, Array Multiplier and Vedic Arithmetic Using VHDL

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doi: https://doi.org/10.21467/proceedings.114.63

Abstract

The multiplication operation is one of the often used operation in many computer and electronic devices. Low power utilization is one of the most essential attributes for meeting several challenges in many applications. In this paper different type of implementation of Booth multiplier has been studied. Multipliers has great importance in digital signal processing, so designing a high speed multiplier is the need the hour. Structures of 4X4 bits Urdhva Tiryagbhya, Nikhilam Sutra have been executed on Spartan 3 XC3S50-5-PQ-208.The determined calculation delay for 4X4 Urdhva Tiryagbhyam was 14.14 ns and force is 20.60 mw. For Nikhilam Sutra the determined computational postponement is 16.16 ns and all out force utilization is 24.60 mw.

Keywords: Booth Multiplier, Array Multiplier, Vedic Arithmetic, DSP, VHDL.

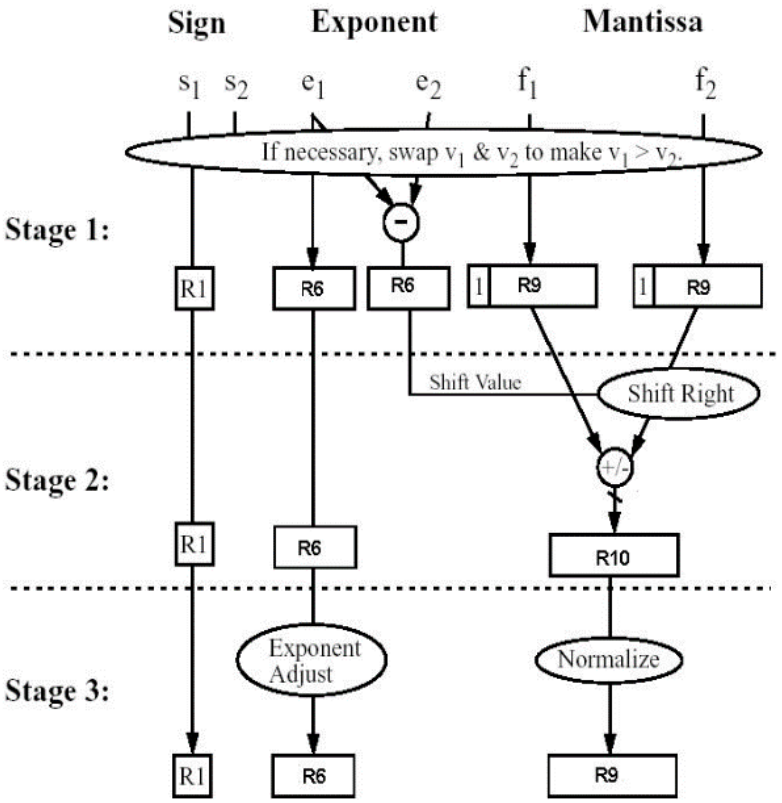
1 Introduction

It is an amazing computation for number augmentation which is marked, it serves both the negative and positive number constantly. It comprises move activity for the standard, there is a creation of one different multiplicand which is added to the midway unit by the multiplier bit. Thus, the k-bit twofold digit may also be decoded as k/2-digit radix-4 digit and a k/3-digit radix-8 digit expansion. Any function performed by digital system is generally went through the measurement of used multiplier [1]. A no responsibility liberal radix-2 booth's recording construction is plotted & developed for Quantum Cost & improvement through Quantum Cost. It is shown by the Garbage Output Multiplier in [2]. The booth radix-4 proves to be the best as it has the least area, power and fastest performance dispatch [3]. The radix-2 booth multiplier still owns largest area and highest time hindrance [4]. The most interpretative blocks contains multiplier. Radix-4 booth multiplier provides higher processing time as compared to conventional multiplier [5]. Multiplier is one of the considerable computation operations switching DSP applications. There is an improvement in he regulation and performance of applications because of their recomposed layout [6]. Last step of multiplier is substituted by proposed adder. Both conventional & proposed multiplier are built in with 16-T full adder [7]. The computation elasticity is improved by matrix amplification in a two spatial working component [8]. Digital multiplier work on the notion of Vedic Math [9]. Many ways are implemented for the improvement in speed of multiplier, the vedic multiplier is at the focal point as it works faster and has low power expenditure [10].

2 Booth Multiplier

Booth multiplier is a spectacular computation for marked number augmentation. The k-bit double digit may also be decrypted as K/2- digit radix-4 digit and a K/3 digit radix-8 digit. It utilizes high radix increase thus it can handle further than the modest bit of multiplier in every cycle. The flow chart of booth multiplier is shown in the Figure 1.

Proceedings DOI: 10.21467/proceedings.114; Series: AIJR Proceedings; ISSN: 2582-3922; ISBN: 978-81-947843-8-8



Rx = x-Bit Register

Figure 1 : Booth Multiplier

2.1 RTL of Booth Multiplier

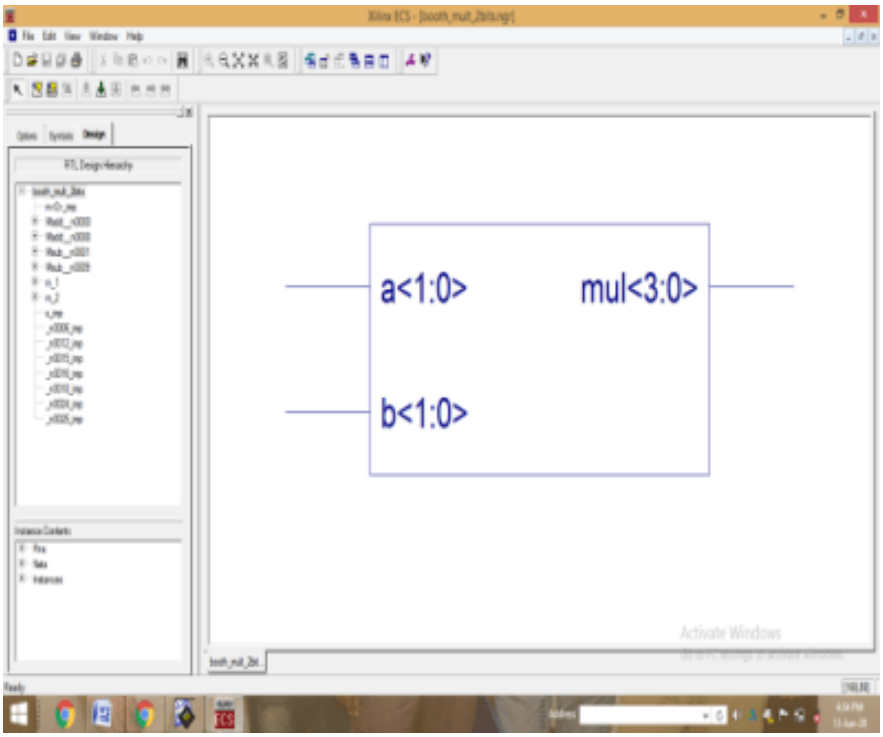


Fig 2 : RTL Booth Multiplier 2bits

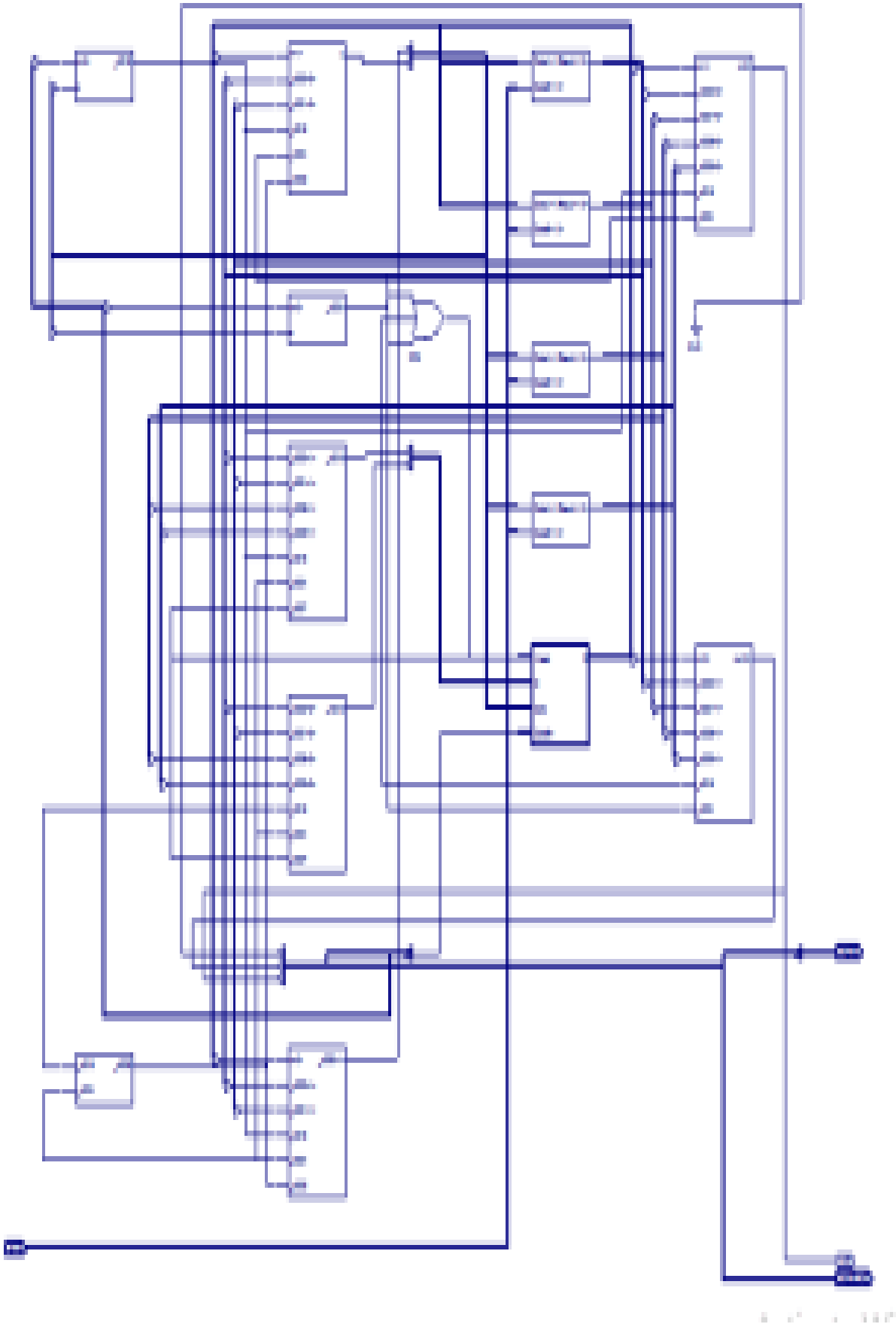


Figure 3: RTL Booth Multiplier

2.2 VHDL Code for Booth Multiplier

```
Library IEEE;
Use IEEE.Std_Logic_1164.all;
Use IEEE.Std_Logic_Arith.all;
Entity Booth_Mult_2bits is
Port(a,b : in Std_Logic_Vector(1 downto 0); mul: out Std_Logic_Vector( 3 downto 0));
End Booth_mult_2bits;
ArchitectureBooth_mult_2bits of Booth_mult_2bits is
Begin
Process(a,b)
Variable m: Std_Logic_Vector(3 downto 0):=”0000”;
Variable s: Std_Logic;
Begin
For i in 1 downto 0 generate
If (m(0) =’0’ and s=’1’ )then
 m(1 downto 0):=”00”+ a;
   s:=m(0);
m(0):=’0’;
elsif(m(0)=’1’ and s=’0’)then
     m(1 downto 0):=”00” –a;
      s:=’0’;
m(0):=’0’;
else
      s:=’0’;
 m(0 downto 0):=m(1);
mult<=m;
end if;
end generate;
end process;
end Booth_mult_2bits;
```

3 Waveform of Multiplier

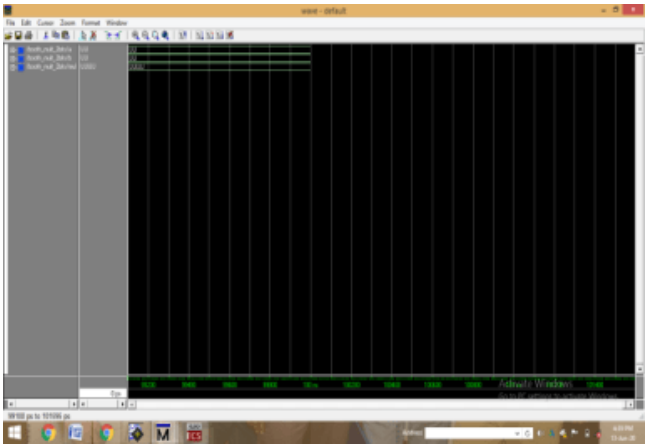


Figure 4: Multiplier

4 Conventional Array Multiplier

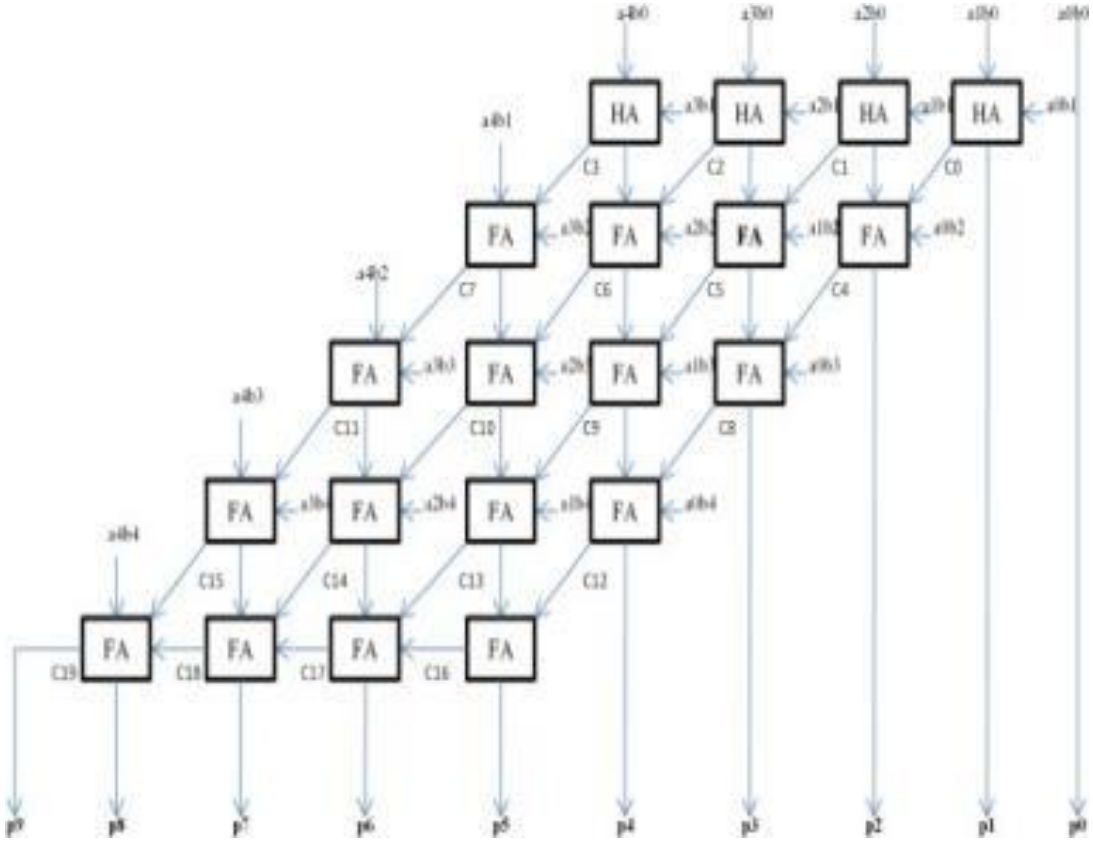


Fig.5: Conventional array multiplier

There is an involvement of AND working of multiplicand & multiplier bits and successive adding in the process of binary array multiplication [3]. There are sixteen full adder and four half adder in conventional array multiplier which is also shown in figure 4.

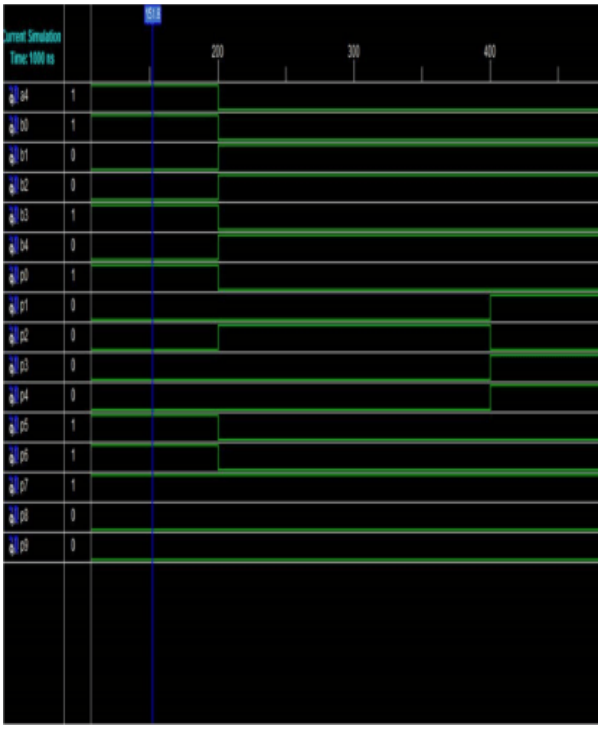


Figure 6: Simulation result of the Array Multiplier.

Table I :-Array Multiplier

Logic Utilization	Conventional Array Multiplier
No. of Pieces	30
No. of 4 input LUTs	52
No. of bonded IOBs	20

5 Vedic Arithmetic

The name Vedic Arithmetic is given to the rediscovery of science done by the Vedas. In contrast with regular science Vedic arithmetic is less difficult and straightforward. Master Bharati Krishna Tirthaji Maharaj. What's more, enormous incomplete entirety and halfway convey registers requires exponential tasks.

Need for Vedic Mathematics

- It diminishes the scratch from finger.
- It expends the less time.
- It is mystical instrument for the counts.
- It give the one-line answer.
- It gives the more focuses to works.

Uses of Multiplier

Multipliers are broadly utilized in

- For convolutions, factorial figuring.
- Arithmetic and rationale unit in processors
- For different numerical activities like establishing, divisions.
- Floating point units.
- FIR channels.
- Speech combination/acknowledgment.
- DSP calculations, for example, FFT DFT.
- Math processors.
- In cryptography.

6 VEDIC MULTIPLICATION

In this paper, the introduced Vedic multiplier is relying upon the Vedic augmentation formulae (Sutras).

7 SIMULATIONS AND RESULTS

The Urdwa Sutra, Nikhliam Sutra can be actualizing on the Xilinx 8.1 and family utilized SPARTAN 3 and gadget XC3S50E the blend report for HDL are appeared as

Proceedings DOI: 10.21467/proceedings.114
ISBN: 978-81-947843-8-8

Series: AIJR Proceedings
ISSN: 2582-3922

Table No. II :- HDL Synthesis Report

Device Spartan 3 XC3S50-5-PQ-208	4x4 Urdwa sutra	4x4 NIKHLIAM SUTRA
Delay	14.14ns	16.16ns
Power consumptions	20.60mw	24.62mw
Number of slices	23 out of 768 (2%)	16 out of 2448 (1%)
Number of inputs LUT	40 out of 1536 (2 %)	29 out of 4896 (1%)
Number of bonded IOBs	17 out of 146 (11%)	16 out of 152 (10%)
Ambient temp.	25 C	25 C
Estimated junctions temp.	26 C	27 C

The waveform for Urdhwa Sutra are appeared as:-

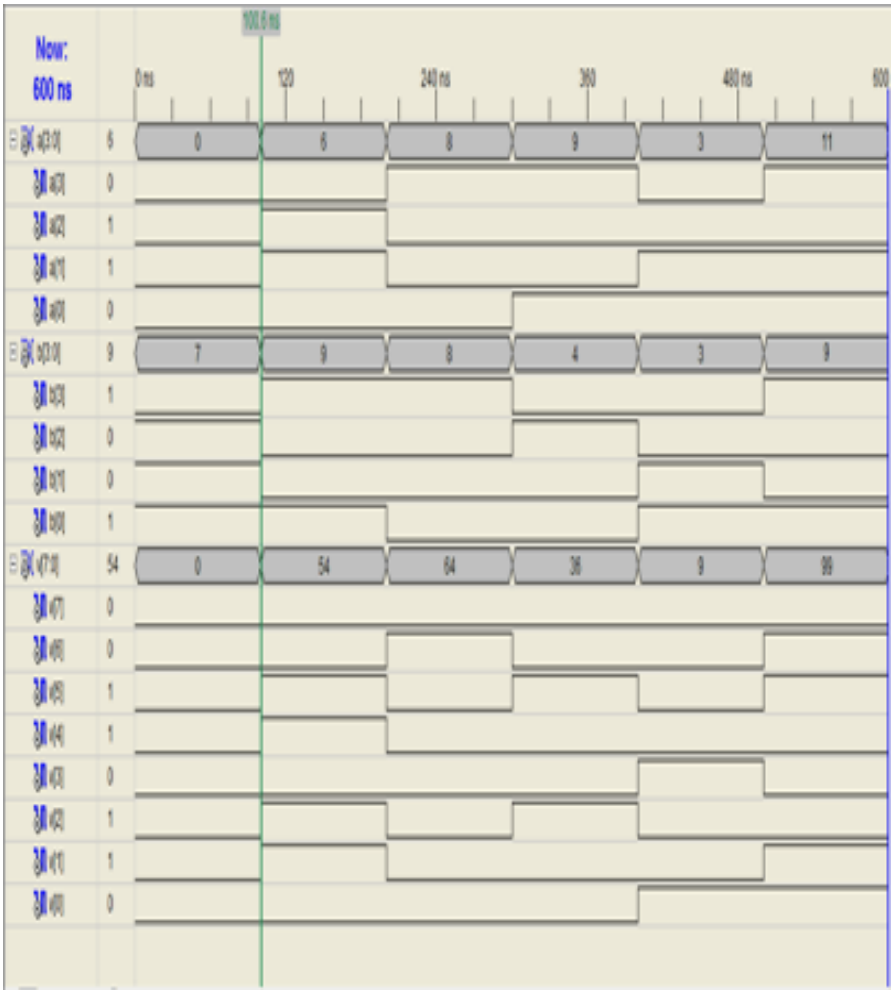


Figure 6: Waveform for Urdwa sutra

The waveform for Nikhliam Sutra are shown as

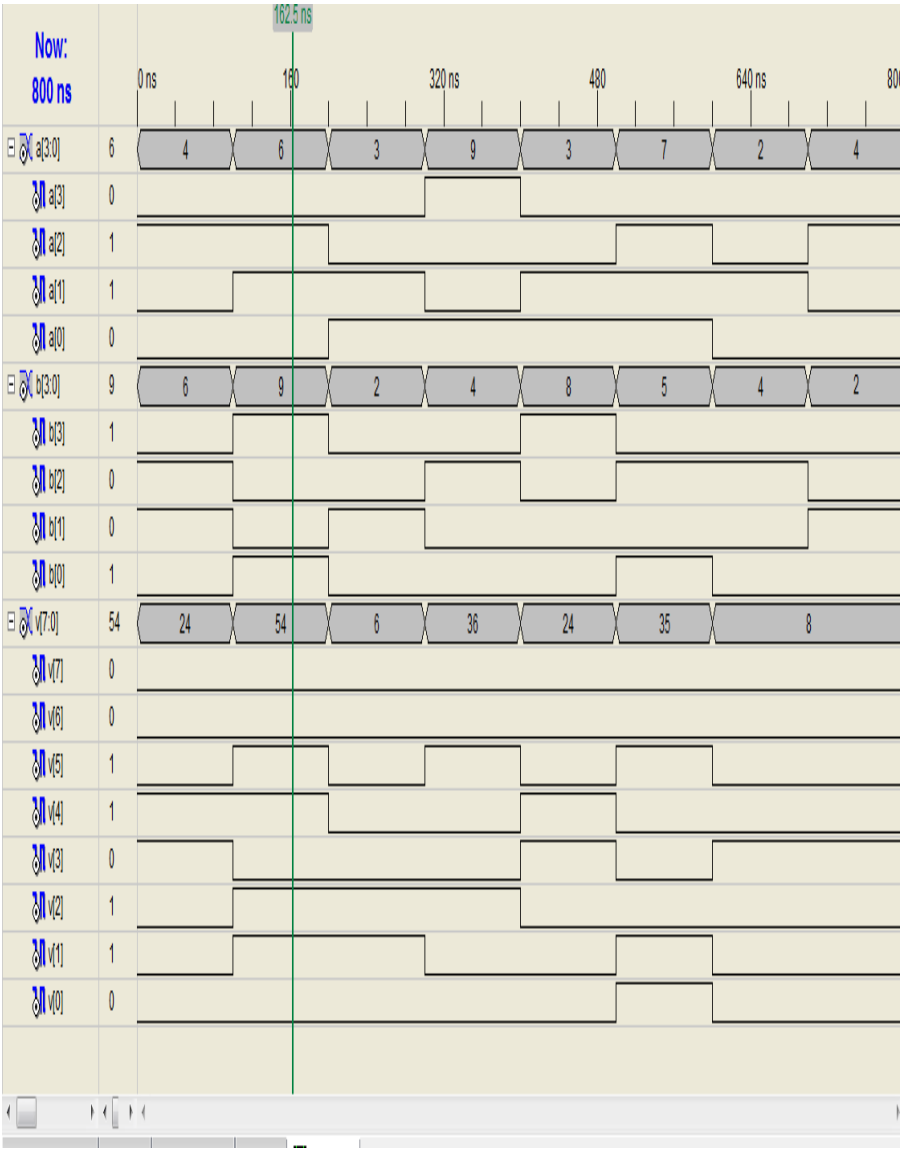


Figure 7 : Waveform for Nikhilam Sutra

Figure 5 shows the simulation result of the array multiplier. In Figure 5, the input is 5x5 bits data and output is 10-bit data. Figure 6 shows the waveform for Urdwa sutra. Figure 7 shows the waveform for Nikhilam Sutra.

8 Conclusion

The above designing of Array Multiplier and Booth multiplier have the simulation of Xilinx(6.1i) stage and has an implementation of Sparton 3. The Booth multiplier has increase in its speed by 61.11% as compared to the Array multiplier with about similar area (LUTs). The Vedic multiplier use additional area compared to the other multipliers, it is two fold faster than other multipliers. The total multiplier delay is 30.30 ns. The Vedic multipliers design from 2x2 to 64x64. The disadvantage in Vedic multiplier can be noticed above binary multipliers. The delay difference varies under span of ns & thus do not influence greatly in circuit.

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ISBN: 978-81-947843-8-8

Series: AIJR Proceedings
ISSN: 2582-3922

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