Design and Simulation of Silicon Nanowire Tunnel Field Effect Transistor

Parveen Kumar*, Balwinder Raj

ECE Department, Dr. B.R. Ambedkar National Institute of Technology, Jalandhar, India

*Corresponding author

doi: https://doi.org/10.21467/proceedings.114.62

Abstract

This paper analyses the different parameters of tunnel field-effect transistor (TFET) based on silicon Nanowire in vertical nature by using a Gaussian doping profile. The device has been designed using an n-channel P^+-I-N^+ structure for tunneling junction of TFET with gate-all-around (GAA) Nanowire structure. The gate length has been taken as 100 nm using silicon Nanowire to obtain the various parameters such as ON-current (I_{ON}), OFF-current (I_{OFF}), current ratio, and Subthreshold slope (SS) by applying different values of work function at the gate, the radius of Nanowire and oxide thickness of the device. The simulations are performed on Silvaco TCAD which gives a better parametric analysis over conventional tunnel field-effect transistor.

Keywords: TFET, Nanowire (NW), Gaussian doping (GD), Subthreshold slope (SS), Drain Current (I_D)

1 Introduction

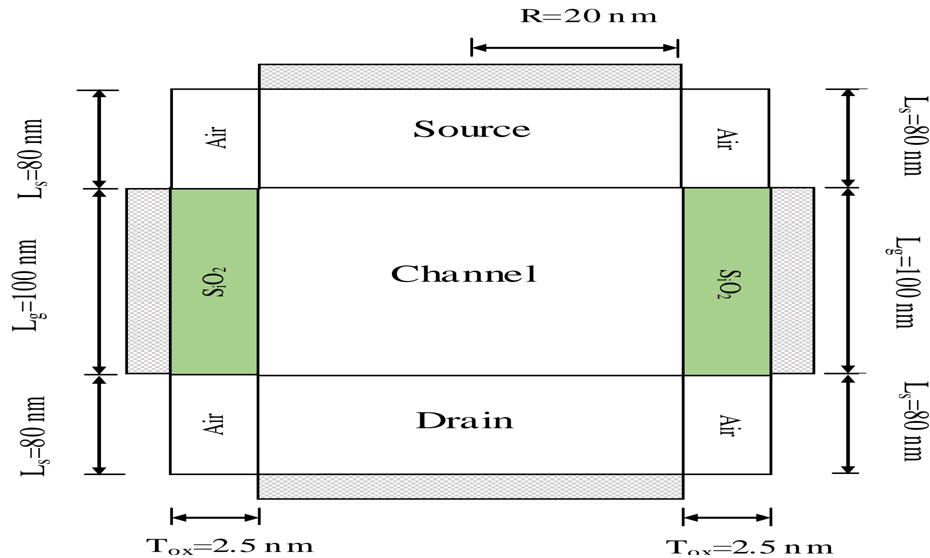
The regular scaling in metal oxide semiconductor field effect transistors (MOSFETs) is very difficult due to various aspects such as current carrier mechanism (thermal emission of electrons); higher short channel effects (SCEs), high OFF current and limited subthreshold slope (60mV/decade) in the Nanoscale regimes [1]–[7]. The main demerit of MOSFET is Subthreshold Slope (SS) which is defined as rate of increase in output (drain) current with the increase in the gate-source voltage (V_{gs}) from 0 volt. The higher SS are effects the supply voltages, which is required for the switching of device from OFF state to ON state [8]–[10]. For the development of new devices in the semiconductor; there is need to be especially low power, lower SS and power efficient device. The tunnel field effect transistor (TFET) is most preferable candidate in the semiconductor industry from the last decade [11]–[15]. The current carrier mechanism of TFET is performed by tunnelling instead of thermionic emission. The structure of TFET is in asymmetrical nature (p-i-n) with different material of source and drain (either n-type or p-type). TFET has number of merits which overcomes the problem of MOSFET such as low Subthreshold slope (SS) which is suitable for low power supply, reduced SCEs [16]–[19] and low OFF-current (I_{OFF}) due to band to band tunnelling mechanism; but it suffers from low ON-current (I_{ON}), which is required for high speed operation of the device. So it should be needed that an advance device which mitigates the problem of low I_{ON} and operating speed. The Nanowire based TFET structures have the potential to gives the better results in terms of high ON-current and higher operation speed with reduced SCEs [20]–[23]. So we have designed and simulate silicon gate all around Nanowire TFET (si-NWTFET) and analyze its various parameters such as I_{ON}, I_{OFF}, ON-OFF current ratio (I_{ON}/I_{OFF}) and SS with the impact of its dimensional parameters such as gate length, oxide thickness and radius of Nanowire.

© 2021 Copyright held by the author(s). Published by AIJR Publisher in the “Proceedings of International Conference on Women Researchers in Electronics and Computing” (WREC 2021) April 22–24, 2021. Organized by the Department of Electronics and Communication Engineering, Dr. B. R. Ambedkar National Institute of Technology, Jalandhar, Punjab, INDIA

Proceedings DOI: 10.21467/proceedings.114; Series: AIJR Proceedings; ISSN: 2582-3922; ISBN: 978-81-947843-8-8

2 Device Structure

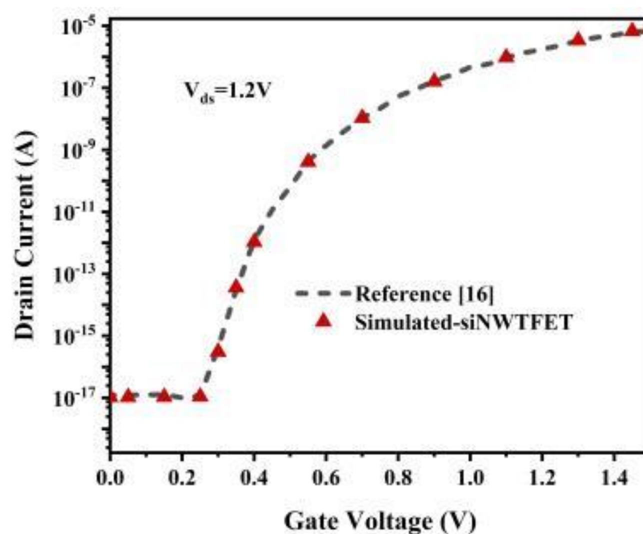
The structure of designed silicon gate all around Nanowrie TFET (si-NWTFET) is shown in Fig. 1. The basic p^+-i-n^+ structure of TFET is used for device designing with Silicon GAA Nanowire. The basic parameters of si-NWTFET taken as gate length (L_g) = 100 nm, Nanowire Radius (R) = 20 nm, Source/Drain length ($L_{s/d}$) = 80 nm, thickness of gate oxide (T_{ox}) = 2.5 nm with Gaussian doping concentration are used for simulation of the device using Silvaco Atlas Tools.



3 Strcture of si-NWTFET.

The high source/drain doping concentration, channel doping concentration and gate-workfunction of siNWTFET are taken as $1*10^{-19}$ cm^{-3}, $1*10^{-17}$ cm^{-3} and 4.3 eV respectively. The Silicon thickness are maintained under Debye-length; as$\sqrt{([(\epsilon_{si} V_T)/q + 60.N])}$, where as q, N, V_T represents the charge of electron, concentration and thermal voltage respectively while ϵ_{si} refer as dielectric constant [24][25].

The proposed structure is calibrated with reported conventional TFET structure [16]. The basic parameters of conventional device are taken same as reported in ref [16]. The calibration has been done using plot digitizer tools and Silvaco Simulation Tool. The calibration curve of siNWTFET is shown in Fig. 2.



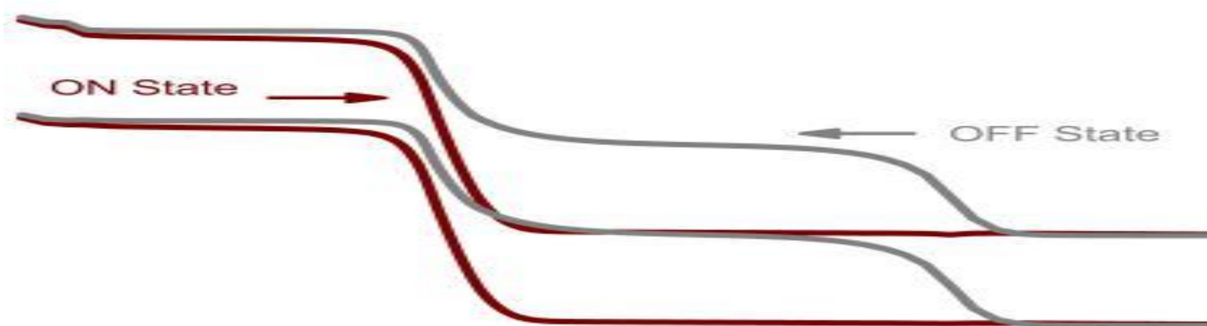
Calibiration Cuve of si-NWTFET with ref [16].

The different models have been used for simulations such as BTBT model for tunneling, BGN model for the effect of bandgap and FLDMOB for field-dependent mobility as well as FERMI model for Fermi–Dirac statistics with the addition of CVT model. The used parameter for siNWTFET designing is illustrating in Table I.

PARAMETER OF SINWTFET

Parameters	Values
Gate length (L_g)	100 nm
Work-function of Gate (ϕ_g)	4.3eV
Thickness of gate oxide (T_{ox})	2.5 nm
Nanowire Radius (R)	20 nm
Channel Concentration	$1 \times 10^{17} cm^{-3}$
Source/Drain Concentration	$1 \times 10^{19} cm^{-3}$

Fig. 3 illustrate the energy band diagrams of si-NWTFET in ON state and OFF state which is performing as tunneling actions during simulation process.



Engery band diagram of siNWTFET.

When the gate voltage is equal to zero and greater than zero (~1.5V), device will act as OFF state and ON state respectively by applying drain-source voltage is 1.0 V. The energy gap between valance band and conduction band is higher in OFF state but lesser in ON state. So the tunneling of electrons has possible only in ON state as shown in energy band diagram.

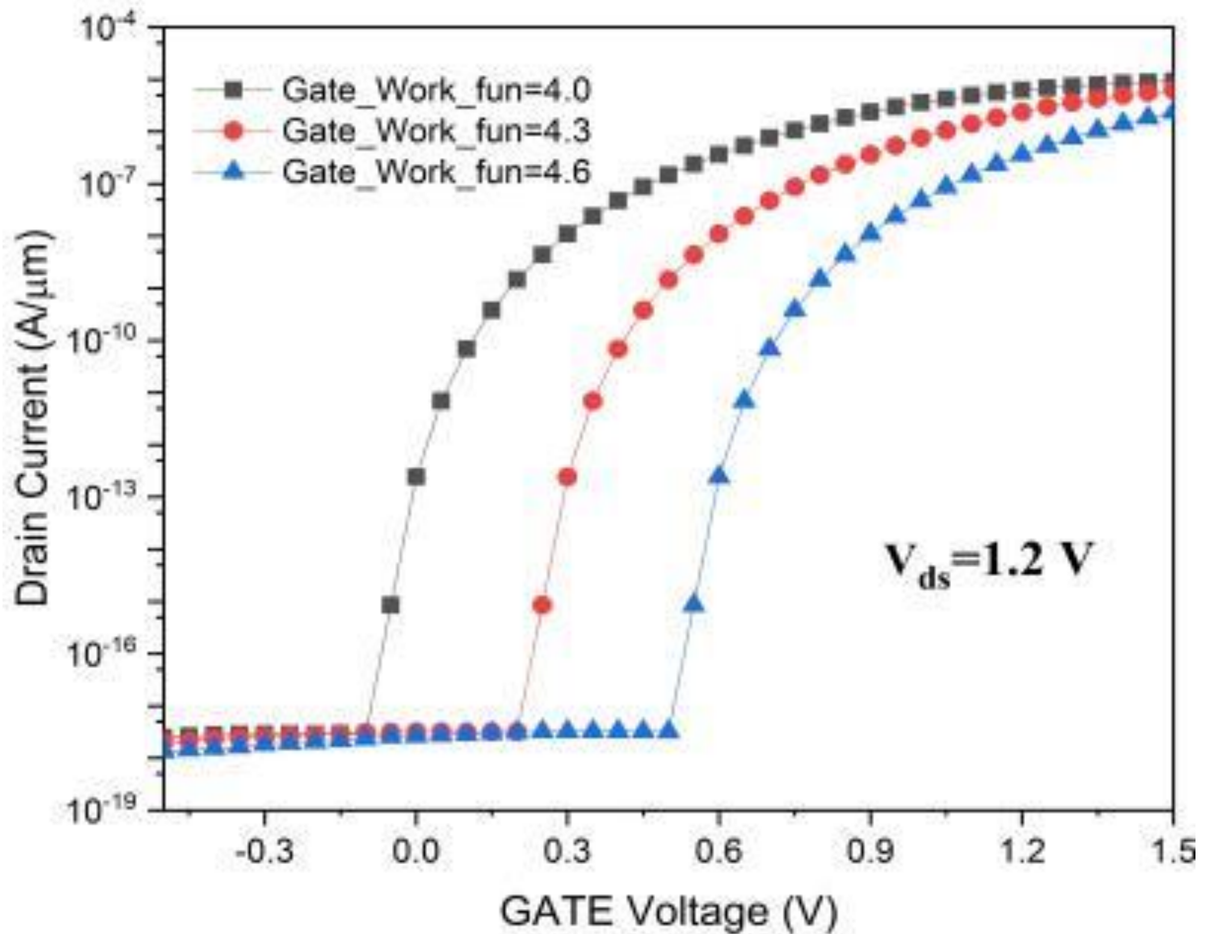
4 Result and Simulation

The result and simulation of si-NWTFET are explained in this section by using Silvaco simulation tool. To calculate the different parameters such as drain current, ON/OFF ratio and SS, dimensional parameters has been varied such as gate work-function (ϕ_g), oxide thickness and radius of Nanowire. The drain current variation of si-NEFET are observed with the effect/impact of different parameters such as

4.1 Effect of work-funtion (ϕ_g)

Firstly, the I_D characteristics are observed with different ϕ_g and taken as 4.0 eV, 4.3 eV and 4.6 eV as shown in Fig. 4. For the simulation work the gate voltage varied from 0 to 1.5 voltage and drain-source voltage (V_{ds}) taken as 1.2V.

Proceedings DOI: 10.21467/proceedings.114
ISBN: 978-81-947843-8-8
Series: AIJR Proceedings
ISSN: 2582-3922

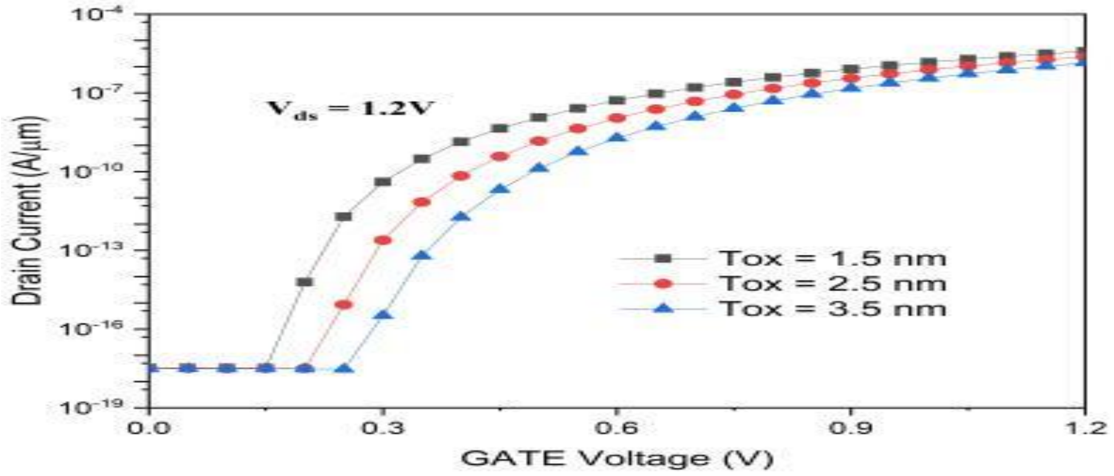


Effect of gate work-function on drain current.

Acording to Fig. 4, the maximum ON current (3.60×10^{-6}) and minimum SS (20.25 mV/dec) are observed at ϕ_g =4.0 eV, but OFF (2.45×10^{-13}) current is also high which leads the SCEs. On the other hand lower OFF current are observed at 4.3 eV. So ϕ_g =4.3 has been taken for proposed device for minimum SCEs.

4.2 Effect of oxide thixkness (T_{ox})

Secondly, the I_D characteristics are observed with different T_{ox} (1.5 nm, 2.5 nm and 3.5 nm). Fig. 5 illustrates the simulation work of siNWTFET on drain current with the impact of different T_{ox} at 1.2V drain-source voltage. It is observed that better parametric value of I_D and current ratio with minimum SS (19.40) at Tox=1.5 nm. During the simulation process ϕ_g , R and T_{ox} has been taken as 4.3 eV, 20 nm and 2.5 nm respectively. The minmum value oxide thickness has given good parametric values and lesser leakgae current in the device.

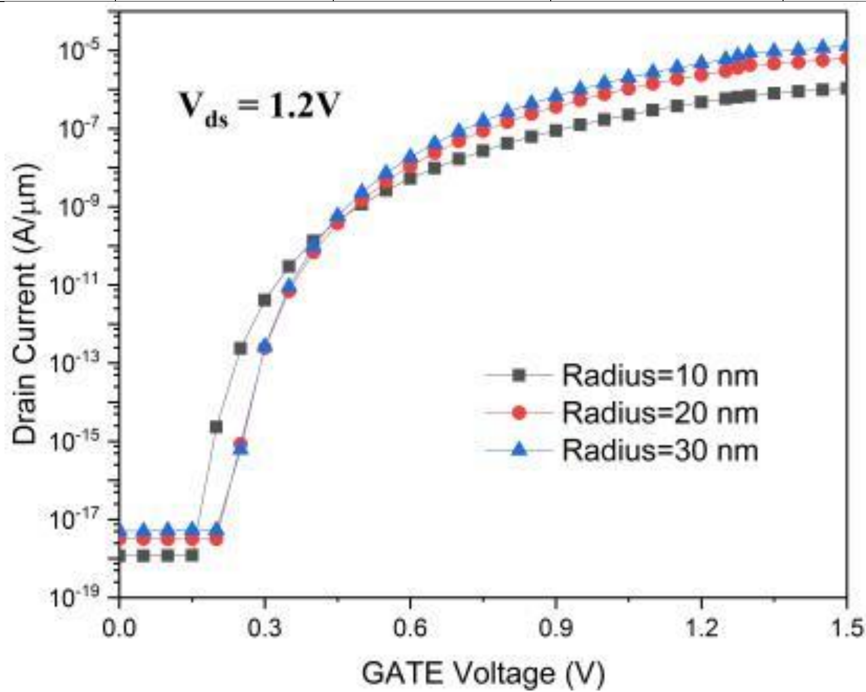


Drain current variation due to effect of T_{ox}.

4.3 Effect of Nanowire Radius (R)

The drain current variation with the effect of nanowire radiu are shown in Fig. 6. According to characteristics curve it observed that higher I_{ON} (1.45×10^{-6}) at R= 30 nm, but the

Parameters	I_{ON} (A/µm)	I_{OFF} (A/µm)	I_{ON}/I_{OFF} Ratio	SS (mV/dec)
ϕ_g = 4.0 eV	3.60×10^{-6}	2.45×10^{-13}	1.47×10^{7}	20.25
ϕ_g = 4.3 eV	7.63×10^{-7}	3.23×10^{-18}	2.36×10^{11}	20.32
ϕ_g = 4.6 eV	4.76×10^{-8}	2.67×10^{-18}	1.78×10^{10}	20.32
T_{ox} = 1.5 nm	2.05×10^{-6}	2.95×10^{-19}	6.94×10^{12}	19.40
T_{ox} = 2.5 nm	1.85×10^{-6}	4.70×10^{-19}	3.94×10^{12}	23.81
T_{ox} = 3.5 nm	1.71×10^{-6}	7.40×10^{-19}	2.31×10^{12}	25.67
R = 10 nm	1.69×10^{-7}	1.17×10^{-18}	1.45×10^{11}	15.22
R = 20 nm	7.63×10^{-7}	3.23×10^{-18}	2.36×10^{11}	20.32
R = 30 nm	1.45×10^{-6}	5.13×10^{-18}	2.83×10^{11}	18.95



Drain current variation due to effect of T_{ox}.

Proceedings DOI: 10.21467/proceedings.114

Series: AIJR Proceedings
ISBN: 978-81-947843-8-8
ISSN: 2582-3922

I_{OFF} current is also at this stage. Due to R variation on siNWTFET the better SS (15. 22) has been archived on 10 nm. During to simulation work, gate voltage is varied from 0 to 1.5 and V_{ds}=1.2. The detailed observed parametric values are given in Table II.

5 Conclustion

The device (si-NWTFET) has been designed and simulated using Gaussian doping profile and analysed parametric variations of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and SS. The simulated results have also showns the effect on drain-current (I_d) with impact of Tox, R and ϕ_g of the device. The most suitable parametric value are observed such as I_{ON} = 3.60x10^{-6} A/μm, I_{OFF} = 2.95x10^{-19} A/μm, SS = 15.22 mV/dec and $I_{ON/OFF}$ = 6.94×10^{12}. The proposed si-NWTFET device structure will be suitable for low power applications.
PARAMETER OF SINWTFET AFTER SIMULATION

6 Acknowledgment

We thank the Group, department of Electronics and Communication Engineering, NIT Jalandhar and VLSI Design Group NITTTR Chandigarh for their interest in this work and useful comments to draft the final form of the paper. The support of SERB, Government of India, and Project (EEQ/2018/000444) is gratefully acknowledged. We would like to thank NIT Jalandhar and NITTTR Chandigarh for lab facilities and research environment to carry out this work.

References

[1] C. Duvvury, "A guide to short-channel effects in MOSFETs," *IEEE Circuits Devices Mag.*, vol. 2, no. 6, pp. 6–10, 1986.

[2] K. P. Cheung, "On the 60 mV/dec@ 300 K limit for MOSFET subthreshold swing," in *Proceedings of 2010 International Symposium on VLSI Technology, System and Application*, 2010, pp. 72–73.

[3] M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, "Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827–834, 2010.

[4] M. Xu *et al.*, "Improved short channel effect control in bulk FinFETs with vertical implantation to form self-aligned halo and punch-through stop pocket," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 648–650, 2015.

[5] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[6] R. Narang, M. Gupta, and M. Saxena, "Investigation of dielectric-modulated double-gate junctionless MOSFET for detection of biomolecules," in *2013 Annual IEEE India Conference (INDICON)*, 2013, pp. 1–6.

[7] Q. Chen, B. Agrawal, and J. D. Meindl, "A comprehensive analytical subthreshold swing (S) model for double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1086–1090, 2002.

[8] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire $ n $-Type Tunneling FETs With Low Subthreshold Swing ($\leq\hbox {50}\\hbox {mV/decade} $) at Room Temperature," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 437–439, 2011.

[9] S. Sharma, B. Raj, and M. Khosla, "Comparative Analysis of MOSFET CNTFET and NWFET for High Performance VLSI Circuit Design," *A Rev. J. VLSI Des. Tools Technol.*, vol. 6, no. 2, pp. 19–32, 2016.

[10] S. K. Sharma, B. Raj, and M. Khosla, "A Gaussian approach for analytical subthreshold current model of cylindrical nanowire FET with quantum mechanical effects," *Microelectronics J.*, vol. 53, pp. 65–72, 2016.

[11] S. Kumar and B. Raj, "Simulations and modeling of TFET for low power design," in *Handbook of Research on Computational Simulation and Modeling in Engineering*, IGI Global, 2016, pp. 640–667.

[12] M. J. Kumar and S. Janardhanan, "Doping-less tunnel field effect transistor: Design and investigation," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3285–3290, 2013.

[13] G. Wadhwa and B. Raj, "Design, Simulation and Performance Analysis of JLTFET Biosensor for High Sensitivity," *IEEE Trans. Nanotechnol.*, vol. 18, pp. 567–574, 2019.

[14] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, 2014.

[15] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, 2007.

[16] Z. X. Chen *et al.*, "Demonstration of tunneling FETs based on highly scalable vertical silicon nanowires," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 754–756, 2009.

[17] N. Kumar and A. Raman, "Performance Assessment of the charge-plasma-based cylindrical GAA Vertical nanowire TFET with Impact of interface trap charges," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4453–4460, 2019.

[18] S. Badgujjar, G. Wadhwa, S. Singh, and B. Raj, "Design and analysis of dual source vertical tunnel field effect transistor for high performance," *Trans. Electr. Electron. Mater.*, vol. 21, no. 1, pp. 74–82, 2020.

[19] M.-C. Sun *et al.*, "Scalable embedded Ge-junction vertical-channel tunneling field-effect transistor for low-voltage operation," in *2010 IEEE Nanotechnology Materials and Devices Conference*, 2010, pp. 286–290.

[20] M. Rahimian and M. Fathipour, "Junctionless nanowire TFET with built-in NPN bipolar action: Physics and operational principle," *J. Appl. Phys.*, vol. 120, no. 22, p. 225702, 2016.

[21] S. Mokkapati, N. Jaiswal, M. Gupta, and A. Kranti, "Gate-all-around nanowire junctionless transistor-based hydrogen gas sensor," *IEEE Sens. J.*, vol. 19, no. 13, pp. 4758–4764, 2019.

[22] S. K. Sharma, A. Jain, and B. Raj, "Analysis of triple metal surrounding gate (TM-SG) III–V nanowire MOSFET for photosensing application," *Opto-Electronics Rev.*, vol. 26, no. 2, pp. 141–148, 2018.

[23] P. Kumar and S. K. Sharma, "Comparative Analysis of Nanowire Tunnel Field Effect Transistor for Biosensor Applications," *Silicon*, pp. 1–8, 2020.

[24] G. Wadhwa and B. Raj, "Parametric variation analysis of symmetric double gate charge plasma JLTFET for biosensor application," *IEEE Sens. J.*, vol. 18, no. 15, pp. 6070–6077, 2018.

[25] T.Chawla, M.Khosla and B.Raj, "Optimization of Double-gate Dual material GeOI-Vertical TFET for VLSI Circuit Design", *IEEE VLSI Circuits and systems Letter*, vol.6, no. 3, pp. 13-25, 2020.

ISBN: 978-81-947843-8-8

ISSN: 2582-3922