# A Temperature-Dependent Threshold Voltage Model for SiGe Source/Drain Si–NT JLFET

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**Abstract**

In this paper, we investigate the impact of temperature on threshold voltage in the SiGe source/drain silicon-nanotube junctionless field effect transistor (NT JLFET). A threshold voltage model has been derived with inclusion of temperature for presented device. It is found that when the temperature increases from $T$ = 300 K, $T$ = 400 K, and $T$ = 500 K, the strain produced by the SiGe source/drain on channel has been relaxed. However, the elevated temperature decreases the potential and the electric field in channel due to increases in intrinsic carrier concentration which further shifts the Fermi level towards the band gap. It has been evaluating that the threshold voltage roll-off and the short channel effects increases due to increases in temperature. The numerical results of threshold voltage model have been well compared with results of 2-D technology computer aided design (TCAD) simulations.

**Keywords:** Drain-induced barrier lowering (DIBL), junctionless (JL) transistor, SiGe source/drain, short channel effects (SCEs).

## 1 Introduction

The continuous demand of high-performance small scale computational devices has been the driving force for aggressive scaling of the metal oxide semiconductor field effect transistor (MOSFET) [1]-[4]. However, the in pursuit of scaling of transistor the short channel effects (SCEs), high leakage current and power dissipation has been increasing at alarming rate [5]. Several multi-gate field effect transistors (MugFET) have been investigated to improve the performance of conventional transistor. Presently, the gate-all-around (GAA) are most promising candidates for ultimate small-scale devices [6]. Due to superior gate control over the channel charge the GAA nanowire field effect transistors (NWFET) have reduced short channel effects and steep subthreshold slope and make them suitable for low power applications [7]. However, the ON-state drive current for GAA NWFETs is of few micro-amperes (μA) and to increase the drive current, NWs have to stacked in arrays which reduced the area efficiency of chip in ultra-large-scale integrations [9]. Therefore, A silicon nanotube architecture has been proposed in [10], which has ultimate short channel immunity and high ON-state drive current. To further improve the performance of the nanotube architecture, A junctionless nanotube field effect transistor has been introduced which has very low leakage current with $I_{ON}/I_{OFF}$ ratio of $10^6$ [8]. Another, NT FET architecture with intrinsic $P^+$ has been proposed to further improve the performance of nanotube FET [11].

However, the nanotube architecture has been studied rigorously for improved drive current capability, there has been very less discussion on temperature analysis of NT FET in literature. A threshold voltage model for double gate all around for ultra-scale nanotube FET has been proposed in [15]. We have already derived the threshold voltage model of SiGe S/D NTJLFET in our previous work [12][13]. Also, we have demonstrated that inclusion of SiGe on source drain side produces the strain in channel which leads to valance band discontinuity. This valance band discontinuity decreases short channel effects with scaling like threshold voltage roll-off, very low leakage current and high drive current capability [14].



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Therefore, in this paper, we have derived a threshold voltage model with inclusion of temperature effect. A 2-D Poisson equation has been solved analytically to obtained expression of potential distribution in channel. The electric field and minimum surface potential also have been derived. An expression of threshold voltage with temperature has been presented. To verify the results of the threshold voltage model, the numerical results are compared with results of TCAD simulation and found in good agreements. The rest of the paper is organized as follows: The device structure and design parameters are discussed in Section II. Section III give the potential distribution model description and electric field followed by threshold voltage model their analysis is presented in Section IV. Finally, conclusions are drawn in Section V.

## 2 Device Structure and Design Parameters

The 2D cross sectional view of SiGe S/D NTJLFET is presented in Fig. 1. (a). In the present transistor the SiGe is used at source and drain side produce the strain in channel. The silicon nanotube channel is sandwiched between the outer gate which act as GAA and inner gate to control the electrostatic charge in channel. The core gate is extended beyond the channel length for full depletion of channel. Furthermore, to realize the nanotube architecture, $HfO_2$ as side wall spacers are used. The gate oxide thickness $t_{ox}$ = 1 nm and channel length $L_g$ =20 nm is used for SiGe S/D NTJLFET device. The nanotube thickness $t_{nt}$ =10 nm and core gate thickness $t_{core}$ =10 nm is same throughout the paper. To fully depleted the channel with high uniform doping $N_d = 1\times10^{19}$ cm$^{-3}$, the work function of 4.8 eV is used in device.

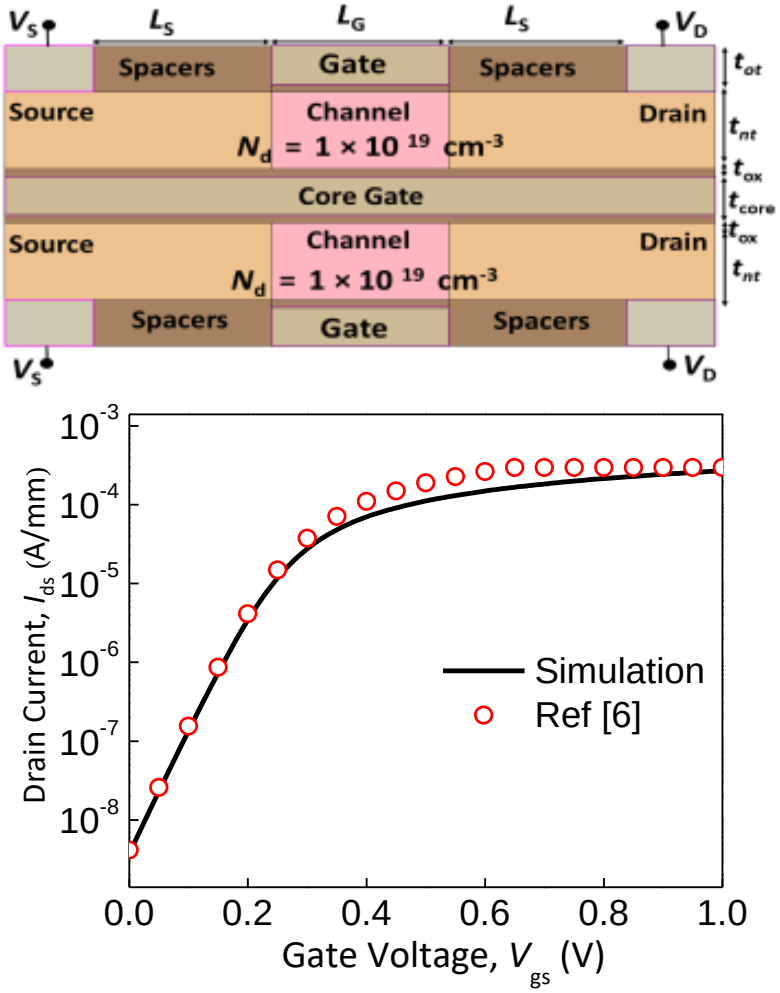


Fig. 1. (a) 2-D cross-sectional view of the SiGe source-drain Si-NT JLFET. (b) Reproducing the results of NW FET to calibrate the simulation set up of [6].

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A systematic 2-D device simulations were performed using Sentaurus TCAD. Philips unified mobility and Lombardi mobility model are incorporated to account for impurity doping and mobility degradation due to electric field. Fermi-Dirac statistics, Shockley-Reed-Hall recombination and Auger recombination models are also invoked for minority combination. Slotboom models is also included to consider the effect of bandgap narrowing to include effect of high doping. To capture the mechanism of L-BTBT, nonlocal BTBT model is also activated. The validation of simulated models that have employed in our work are well calibrated with experimental work in [6] as shown in Fig.1 (b). The simulative results are in good agreement with numerical results indicating that our simulative work efficiently capture the effect of temperature in SiGe S/D NTJLFET.

## 3 Model Description

The gate work function has direct impact on flat band voltage in-turn aberrate the device performance the aberrated flat band voltage with change in germanium content $x$ is formulated as

$$(\Delta E_{\mathrm{C}})_{\mathrm{Si-NT}} = 0.57x,\ (\Delta E_{\mathrm{g}})_{\mathrm{Si-NT}} = 0.4x \tag{1}$$

$$V_{\mathrm{T}} \ln\left(\frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,Si-NT}}}\right) = V_{\mathrm{T}} \ln\left(\frac{\mathrm{m}^{*}_{h,\mathrm{Si}}}{m^{*}_{h,\mathrm{Si-NT}}}\right)^{3/2} \approx 0.075x \tag{2}$$

$(\Delta E_{\mathrm{C}})_{\mathrm{Si-NT}}$ is the increase in electron affinity of Si caused by strain, $(\Delta E_{\mathrm{g}})_{\mathrm{Si-NT}}$ is the decrease in energy bandgap of Si due to strain, $N_{\mathrm{V,Si}}$ and $N_{\mathrm{V,Si-NT}}$ are the density of states (DOS) in the valence band of normal and strained silicon, $\phi_{\mathrm{M}}$ is the gate work function and $\phi_{\mathrm{Si}}$ is the Si work function.

*Potential Distribution*

The potential distribution in channel is calculated using 2-D Poisson's equation in cylindrical coordinates system which is expressed as

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial}{\partial r}\varphi_i(r,z,T)\right] + \frac{1}{r^2}\frac{\partial^2}{\partial r^2}\varphi_i(r,z,T) + \frac{\partial^2}{\partial z^2}\varphi_i(r,z,T) = -q\frac{N_d}{\varepsilon_{si}}\left[\exp\left(\frac{\varphi_i(r,z,T)-V}{U_T}\right)-1\right] \tag{3}$$

Where $i = 1$ for inner gate and $i = 2$ for outer gate.

Equation (3) can be solved by employing superposition technique which decouples the (3) into two parts and can be written as

$$\varphi_i(r,z,T) = W_i(r,T) + V_i(r,z,T) \tag{4}$$

With $W_i(r,T)$ and $(V_i(r,z,T))$ are solution of 1-D Poisson equation and 2-D Laplace equation, respectively. However, equation (3) can be rewritten as

$$\frac{\partial^2}{\partial r^2}W_i(r,T) + \frac{1}{r}\frac{\partial}{\partial r}W_i(r,T) = -q\frac{N_d}{\varepsilon_{si}}\left[\exp\left(\frac{W_i - V}{V_T}\right)-1\right] \tag{5}$$

$$\frac{\partial^2}{\partial r^2}V_i(r,z,T) + \frac{1}{r}\frac{\partial}{\partial r}V_i(r,z,T) + \frac{\partial^2}{\partial z^2}V_i(r,z,T) = 0 \tag{6}$$

Equation (5) is solved by using Chamber's variable transformation technique in [15] and the electric flux

$$Q_i = -\varepsilon_{si}\frac{\partial}{\partial r}W_i(r,T)\Big|_{r=r_i} = C_{OXi}\left(W_i(r,T) - (V_{gs} - V_{\mathrm{fb}})\right) \tag{7}$$

$$W_i(r,T) = V_{gs} - V_{\text{fb}} + C_{r_i} + V_T - 2V_T \text{L}\left( \frac{C_{r_i} r_i \sqrt{2\gamma}}{4V_T} e^{\left(\frac{V_{gs}-V_{\text{fb}}+C_{r_i}-V}{2V_T}\right)} \right) \quad (8)$$

Where $\gamma = qN_d / \varepsilon_{Si} V_T$ and $C_{r_1} = 4\varepsilon_{Si} V_T / r_1 C_{OX1}$. However, the oxide capacitance is $C_{OXi} = \varepsilon_{ox}/t_i$ and $t_i = r_i \ln\left(1 + t_{ox}/r_i\right)$ with $i$=1 for core gate and $i$=2 for outer gate. $r_1 = t_{core} + t_{ox}$ and $r_2 = t_{core} + t_{ox} + t_{nt}$.

The flat band voltage is given by

$$V_{\text{fb}}(T) = \phi_{\text{M}} - \phi_{\text{Si}} - \frac{(\Delta E_{\text{C}})_{\text{Si-NT}}}{q}\phi_{\text{M}} + \frac{(\Delta E_{\text{g}})_{\text{Si-NT}}}{q} - V_{\text{T}} \ln\left( \frac{N_{\text{V,Si}}}{N_{\text{V,Si-NT}}} \right) \quad (10)$$

Where $\phi_{\text{M}}$ and $\phi_{\text{Si}}$ are gate electrode work function and silicon material work function.

And equation (6) has solution

$$V_i(r,z,T) = \sum_{n=1}^{\infty} J_0(\lambda_n r)\left[ A_n \exp(\lambda_n z) + B_n \exp(-\lambda_n z) \right] \quad (11)$$

$A_n$, $B_n$, $C_n$ and $D_n$, are calculated using boundary condition in our previous work [14]. $J_0$ and $J_1$ are Bessel functions with order 0 and 1.

The resultant solution for potential distribution in channel is given by

$$\varphi_i(r,z,T) = V_{gs} - V_{\text{fb}} + C_{r_i} + V_T - 2V_T \text{L}\left( \frac{C_{r_i} r_i \sqrt{2\gamma}}{4V_T} e^{\left(\frac{V_{gs}-V_{\text{fb}}+C_{r_i}-V}{2V_T}\right)} \right) + \sum_{n=1}^{\infty} J_0(\lambda_n r)\left[ A_n \exp(\lambda_n z) + B_n \exp(-\lambda_n z) \right] \quad (12)$$

### 3.1 Electric Field

Furthermore, the $E_1$ and $E_2$ are electric field for core gate and outer gate which are given by

$$E_i = -\frac{\partial}{\partial z}\varphi_i(r,z,T) \quad (13)$$

$$E_i = -\sum_{n=1}^{\infty} \lambda_n \frac{1}{\sinh(\lambda_n L_g)} \left[ \left\{ V_{bi} - \left( V_{gs} - V_{\text{fb}} + C_{r_i} + V_T - 2V_T \text{L}\left( \frac{C_{r_i} r_i \sqrt{2\gamma}}{4V_T} e^{\left(\frac{V_{gs}-V_{\text{fb}}+C_{r_i}-V}{2V_T}\right)} \right) \right) \right\} \times \left( \cosh(\lambda_n z) + \sinh(\lambda_n z) \right) - V_{ds} \cosh(\lambda_n z) \right] \quad (14)$$

### 3.2 Threshold Voltage Model ($V_{th}$)

In general, it is the gate voltage, $V_{\text{gs}}$ at which current conduction start from source side to drain side through a partially depleted channel at minimum potential $\varphi_{\text{s,min}}(r)$. The Vth is calculated when the minimum potential is equal to the Fermi potential in channel. Therefore, using (13) minimum potential can be calculated as in [14]

$$\varphi_{\text{s,min}}(r,T) \approx V_1(r,T) + 2J_0(\lambda_n r)\sqrt{A_n B_n} \quad (15)$$

And

$$\varphi_{s,\min}(r,T)\Big|_{V_{gs}=V_{th}} = V_F(r,T) \tag{16}$$

By solving

$$k_1(V_{th}-S_n)^2 + k_2(V_{th}-S_n) + k_3 = 0 \tag{17}$$

The $V_{th}$ is calculated as

$$V_{th}(T) = S_n + \left(\frac{-k_2 + \sqrt{k_2^{\,2} - 4k_1k_3}}{2k_1}\right) \tag{18}$$

$$k_1 = -\sinh^2(\lambda_n L_g) - 2\sinh(\lambda_n L_g) - 2 \tag{19}$$

$$k_2 = 2(2V_{bi} + V_{ds})\sinh(\lambda_n L_g) + 4V_{bi} \tag{20}$$

$$k_3 = 2(V_{bi}^2 + V_{bi}V_{ds})\sinh(\lambda_n L_g) - V_{bi} - (V_{bi} + V_{ds})^2 \tag{21}$$

$$S_n = V_{fb} - \frac{qN_d}{\varepsilon_{Si}}\left(\frac{t_{nt}^2}{4} - \frac{t_{nt}}{C_{OXeff1}} - r_c^{\,2}\right) \tag{22}$$

## 4 RESULTS AND DISCUSSION

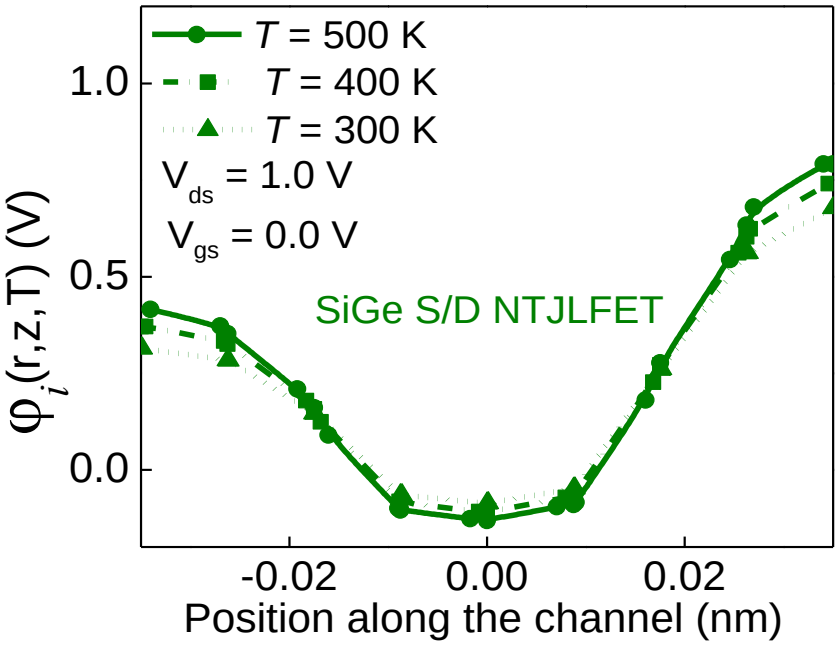


Fig. 2. Potential distribution of channel along the position of channel in SiGe S/D NTJLFET.

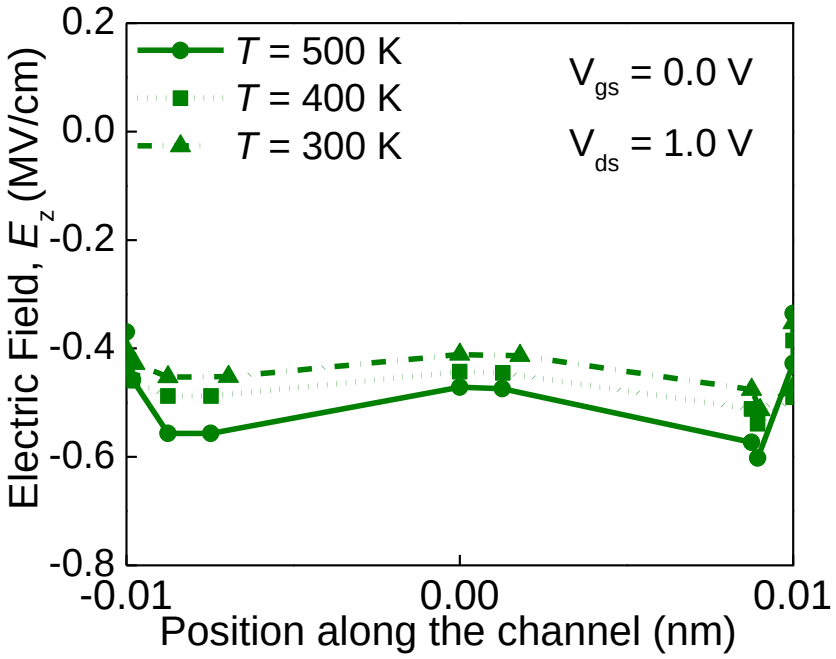


Fig. 3. Electric Field in channel along the position of channel in SiGe S/D NTJLFET.

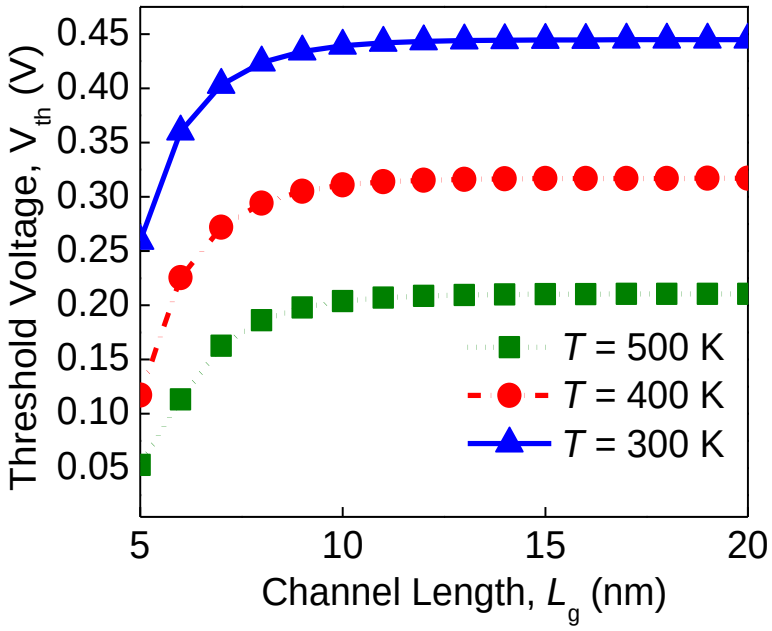


Fig. 4. Threshold voltage with channel length for different temperature.

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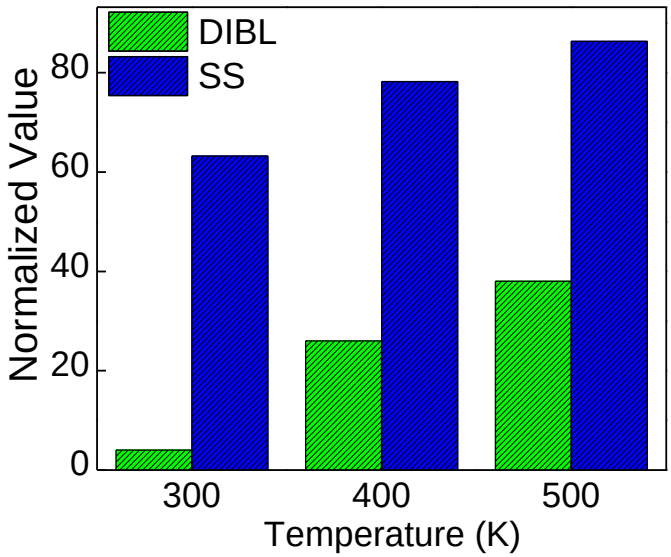


Fig. 5. DIBL and SS at different temperature.

Fig. 2. shows the potential distribution in channel for SiGe S/D NTJLFET at different temperatures, $T$ = 300 K, $T$ = 400 K, and $T$ = 500 K at $V_{ds}$ = 1 V and $V_{gs}$ = 0.0. As the temperature increases the intrinsic carrier concentration increases which reduced the potential in channel. The increases in temperature increases the mobility in channel thus, by shifting the fermi level towards the band gap.

In Fig. 3. the electric field profile is shown with different temperature $T$ = 300 K, $T$ = 400 K, and $T$ = 500 K at $V_{ds}$ = 1.0 V and $V_{gs}$ = 0.0. As it can seen from figure that, with increases in temperature the electric field in the channel decreases due to shift in fermi level towards the band gap. The electric field at drain side lower as it is required for decreased OFF-state current in device.

Furthermore, the Threshold voltage $V_{th}$ of SiGe S/D NTJLFET is shown in Fig. 4. for different temperatures $T$ = 300 K, $T$ = 400 K, and $T$ = 500 K at $V_{ds}$ = 1.0 V and $V_{gs}$ = 0.0. It is clearly seen from the figure that as temperature increases the $V_{th}$ decreases with channel length variation. This is mainly due to relaxation of strain in channel with increase in temperature. The SiGe S/D structure exhibits the better short channel immunity with scaled dimension of NTJLFET device. Fig. 5 shows the DIBL and SS for SiGe S/D NTJLFET for different temperatures. The DIBL and SS are tending to increase with rise in temperature due to relaxed strain in channel. The DIBL and SS increases 58% and 79% for temperature $T$ = 500 K.

## 5 Conclusion

In this paper, A threshold voltage model has been derived with inclusion of temperature using 2-D Poison equation with superposition technique to decouples the potential distribution in channel. We demonstrate that the increases in temperature from $T$ = 300 K, $T$ = 400 K, and $T$ = 500 K, the relax the strain in the channel which is produced by SiGe on source and drain side of silicon nanotube. This produced the valence band discontinuity in channel which increase the SCEs immunity of SiGe S/D NTJLFET with scaling. However, the increase in temperature increases the SCEs due to strain relaxation in channel. The DIBL is 58% higher and the SS is 79% higher for $T$ = 500 K, which is quite increase of SCEs due to temperature elevation. Therefore, it is summarized that the increases of temperature in the SiGe S/D NTJLFET, the performance of device degrades in-terms of high DIBL and SS.

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